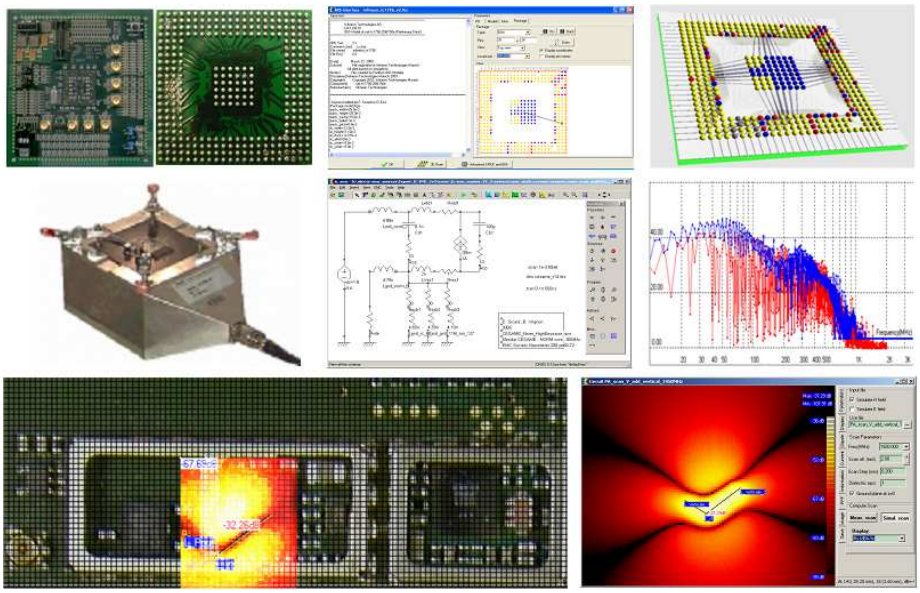
IC-EMC

User's Manual

Version 2.5



www.ic-emc.org

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- The software IC-EMC can be downloaded from www.ic-emc.org
- The companion SPICE simulator WinSpice can be downloaded on a shareware basis from www.winspice.com

About the Authors

Etienne SICARD was born in Paris, France, June 1961. He received the B.S degree in 1984 and the PhD in Electrical Engineering from the University of Toulouse, in 1987, in the laboratory LAAS of Toulouse. He was granted a Monbusho scholarship and stayed 18 months at Osaka University, Japan (1988-1989). Previously a professor of electronics in the Department of Physics, University of Balearic Islands, Spain (1990), Etienne SICARD is currently a professor at INSA of Toulouse, France, Department of Electrical and Computer Engineering. He is a visiting professor at the electronic department of Carleton University, Ottawa, in 2004. His research interests include several aspects of integrated circuits (ICs) for improved electromagnetic compatibility (EMC), and speech processing applied to speech therapy.
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Abstract

This manual document describes the tool IC-EMC (acronym for Integrated Circuit Electromagnetic Compatibility) which aims at simulating parasitic emission and susceptibility of integrated circuits and eases the comparison with measurements. The tool uses the freeware WinSpice derived from SPICE Berkeley for analog simulation.

The context of EMC is illustrated in Chapter 1, with a presentation of the general flow for EMC prediction. The chapter 2 is dedicated to an overview of the software and its main features through several case studies. The third chapter is dedicated to the basic concepts, with a review of specific units, Fourier Transform, conductor model, LC resonance, impedance, transmission line effects, matching, power and S parameters. In chapter 4, the IBIS standard is described, as well as its extension to package construction in 3D. Chapter 5 presents the generic flow for comparing measurements with simulations. The ICEM model, standard macromodel aiming at predicting parasitic level emission, is also presented in this chapter, together with an ICEM model generator. Also in chapter 5, conducted emission simulation and comparison with 1/150Ω measurements are proposed, while chapter 6 concerns the near field radiated emission simulation. Immunity is addressed in chapter 7, starting with the power units, details on the coupler, and simple test cases on unmatched load injection. The Direct Power Injection standard is also described, and simulated. Measurement results are compared to simulations, followed by two case studies including emission and susceptibility measurement and simulation comparison. The chapter 8 provides a serie of links on the IC-EMC website (www.ic-emc.org) about various real case studies of IC modeling for EMC.

The last part of the manual includes a reference section and several appendixes related to interface formats, configuration files, details on the EMC Model library, S parameter deembedding theory, interconnect parameter formulations, and details on the package model extraction using the PEEC method.

The authors have dedicated around two years to build the technical contents of this manual and software, and tried their best to improve the IC-EMC tool, trying to keep the usage simple. As the tool is in constant evolution, we encourage the reader to download the updated version of IC-EMC form the web page and we would appreciate feedback and comments.

Acknowledgements

We would like to thank partners from the Medea+ “Parachute” and Pidea+ “EMCPack” European project for invaluable help in EMC expertise at integrated circuit level. The tools have benefited from the real-case experiments conducted in partnership with ST-Microelectronics Grenoble, France, Freescale Semiconductors, Toulouse, France, Infineon, Munich, Germany, Valeo Créteil, France, and Atmel Nantes France. The development of IC-EMC version 2.5 has also been supported by Aerospace Valley project EPEA.

Toulouse, October 13, 2011

Etienne Sicard, Alexandre Boyer

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1 EMC of Integrated Circuits

1.1 Introduction

Electromagnetic compatibility (EMC) is a fundamental constraint that all electric or electronic equipments must meet to ensure the simultaneous operation of all nearby electric or electronic devices and the safety of users for a given electromagnetic environment (Fig. 1-1). By definition, EMC covers two complementary aspects: the electromagnetic emission and the susceptibility to electromagnetic interferences. The role of an EMC engineer is to reduce both the emission and the susceptibility of an electronic device such that it complies with EMC limits defined by standards, e.g. CISPR25 described in figure 1-2 [1-1].

Figure 1-1 : Illustration of electromagnetic compatibility in a system which embeds electric and electronic devices [1-2]

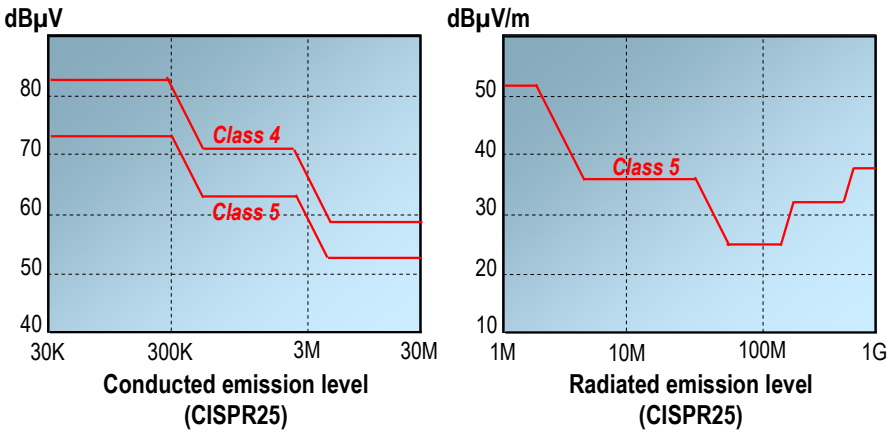

Figure 1-2: Example of standard emission level limit (CISPR25) [1-1]

EMC has been taken into account at system, cable and printed-circuit board (PCB) levels for a long time. Figure 1-3 presents several techniques used to improve EMC of an electronic system.


EMI shielding

Cable shielding


Ferrite beads

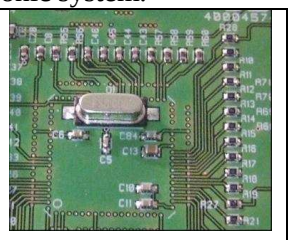
Decoupling capacitors

Figure 1-3 : Different techniques used at system, cable and PCB level to overcome EMC problems

However, considering only EMC at system level is not satisfactory enough. Semiconductor devices are often the source as well as the victim of electromagnetic interferences [1-2]. Possible mechanisms for coupling of electromagnetic noise at integrated circuit (IC) level include the wire connections such as the supply lines, the coupling of the package leads to electric or magnetic field, or even the coupling of the field directly to the silicon chip (Fig. 1-4). Also represented in the figure are couplings through cables and PCB tracks.

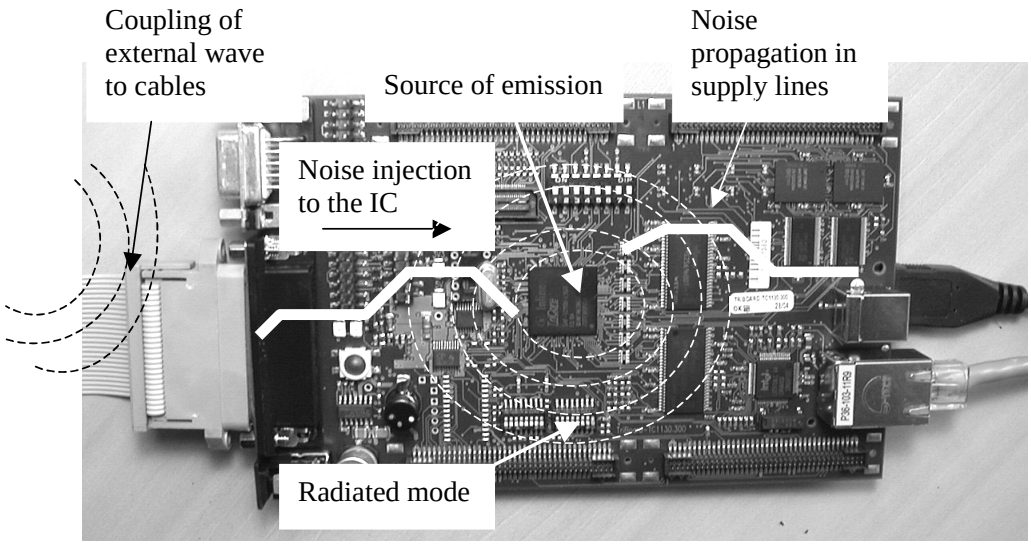

Figure 1-4 : Conducted, radiated emission and susceptibility of an integrated circuit

EMC improvement techniques at system levels, as those presented in Fig. 1-3, are mainly related to noise filtering. Ensuring EMC at circuit level allows an effective reduction of noise sources and disturbance origins. It can also reduce EMC compliance costs by removing some EMC protection devices. In addition, the optimization of selection and placement of EMC protection devices requires an accurate modelling of all the system. As IC is the center part of EMC issues, its modelling cannot be neglected and specific models of ICs must be developed.

1.2 Emission of integrated circuits

1.2.1 Basic mechanisms of electromagnetic emission

Parasitic emission is first caused by the switching activity of integrated circuits (ICs) which induce transient current circulation within the circuit and its direct environment (PCB, cables), as shown on figure 1-5. However, transient current itself do not produce directly electromagnetic interferences. Suppose ideal power supply and ground voltage references, voltages would remain constant whatever the consumed current. In practice, the IC is connected to a non-ideal voltage reference (battery, voltage regulator, ground plane) through interconnections formed by package leads, PCB tracks and cables.

However, these interconnections are not perfect conductors, due to several parasitic effects, represented by electrical elements such as resistor, inductor, and capacitor. Consequently, interconnects can not be considered as equipotential. Thus the wires can convert the transient currents into voltage drops on power and ground supplies (Fig. 1-6). Parasitic inductances of interconnections are the main responsible of voltage drops [1-3]. Conversion of transient current to voltage bounces by inductances is given by equation 1-1. Voltage drops may propagate to circuit sharing the same supply network, which is called *conducted emission*. Moreover, current flows and voltage drops along interconnections generate electromagnetic fields which are responsible of *radiated emission*.

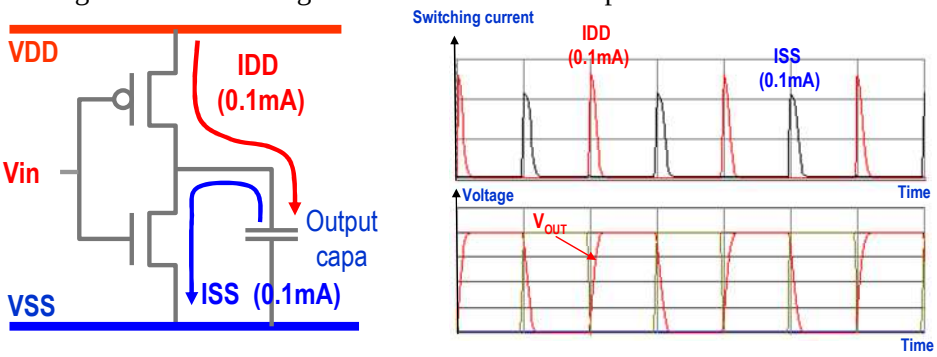

Figure 1-5 : Basic mechanisms of CMOS circuit current – inverter example

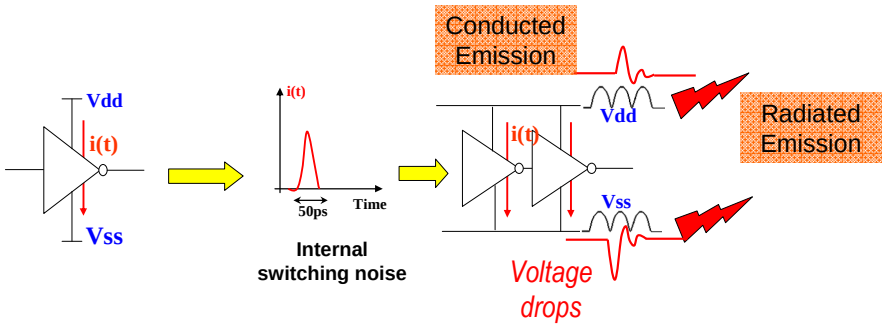

Figure 1-6 : IC parasitic emission due to switching activity and parasitic power supply interconnections

$$\Delta V = L\frac{\Delta i}{\Delta t} \qquad \textit{Equ. 1-1}$$

Influent circuit parameters	Comments
IC internal activity	The Internal Activity (IA) generates a parasitic transient current which flows within the circuit. Thus, a large digital core or parallel I/O buses generate a strong emission because of frequent charge/discharge cycles.
Load connected to the circuit	A large capacitive load induces significant charge transfers and hence parasitic emission.
Filtering effect of the circuit	Interconnections, on-chip decoupling capacitor and parasitic coupling paths have an influence on propagation of parasitic current flow within a circuit. They can contribute to keep parasitic current flow internal to the circuit and reduce supply voltage fluctuations in the best case, or create leakage paths which can disturb sensitive blocks.

Table 1-1: Influent circuit parameters on electromagnetic emission

The electromagnetic emissions of many circuits originate from mechanisms listed in table 1-1. The knowledge of these influent parameters helps to propose emission reduction techniques.

1.2.2 Influence of IC technological evolution on emission

Parasitic emission caused by the switching activity of integrated circuits (ICs) has increased in importance with the tremendous progress in Complementary Metal-Oxide Semiconductor (CMOS) technology. According to the International Technology Roadmap for Semiconductors (ITRS) [1-4], the 32-nm CMOS process will be made available for production in 2010, featuring a standard operating frequency near 50 GHz for processing units, and the capability to integrate within a 3 x 3 cm silicon nearly one billion devices (Table 1-2). When switching, each gate generates a small current pulse which flows mainly on the supply lines. The addition of these elementary current pluses provokes enormous current flows within the chip, close to 100 A in the latest generation of high performance micro-processors. Table 1-3 presents the evolution of several digital circuit characteristics which influence directly EMC performances:

- the power supply voltage, both transient current and noise margin depends on power supply voltage.
- the gate density and the current peak per gate. Even if the current peak produced per gate has continuously been reduced, the gate density and circuit complexity increase.
- the capacitance per gate. The sum of the gate, interconnect and junction capacitances constitutes an intrinsic decoupling capacitance which helps to filter the internal noise.

Year	**2002**	**2007**	**2010**
CMOS Technology	0.12 µm	65 nm	32 nm
Internal Supply Voltage	1.2 V	1.0 V	0.75 V
Max Area (mm²)	22x22	25x25	30x30
Interconnect Layers	7	9	12
Typ CPU Frequency (GHz)	2	20	50
Max number of Pads	1800	2500	5000
EMC			
Conducted Emission (dBµV)	80	90	100
Existing meas. methods	TEM, 1 ohm	GTEM	GTEM
Frequency range of interest: DC to	3 GHz	10 GHz	20 GHz
I/O Modeling	IBIS v3	IBIS v4	IBIS v5
Core Modeling	ICEM	ICEM xHF	unknown

Table 1-2: The increase in EMI with the CMOS technology scale-down

Technology	**Supply**	**Gate density (/mm²)**	**Gate current peak (mA/gate)***	**Capacity (fF/gate)**
1.2 µm (1985)	5 V	8 K	1.1	60
0.8 µm (1990)	5 V	15 K	0.9	40
0.5 µm (1993)	5 V	28 K	0.75	30
0.35 µm (1995)	5-3.3 V	50 K	0.6	25
0.25 µm (1997)	5-2.5 V	90 K	0.4	20
0.18 µm (1999)	3.3-2.0 V	160 K	0.3	15
0.12 µm (2001)	2.5-1.2 V	240 K	0.2	10
90 nm (2004)	2.5-1.0 V	480 K	0.1	7
65 nm (2006)	2.5-0.7 V	900 K	0.07	5
45 nm (2008)	1.8-0.8 V	2000 K	0.05	3
32 nm (2010)	1.8-0.8 V	3000 K	0.04	2

* Fan out = 1 and short interconnects

Table 1-3: Impact of technological scale-down on digital circuit characteristics which have an influence on electromagnetic compatibility [1-5]

Due to these transient currents, the ICs may generate conducted and radiated parasitic emission. The increase in operating frequencies, circuit complexity and number of I/Os is depicted in table 1-2, according to the EDA roadmap [1-5]. It can be seen that the peak emission level also tends to increase,

and may provoke severe interference inside and near the IC. Most measurement methods are limited to 1 GHz. The GTEM measurement method, applicable to radiated emission up to 18 GHz, is under standardization.

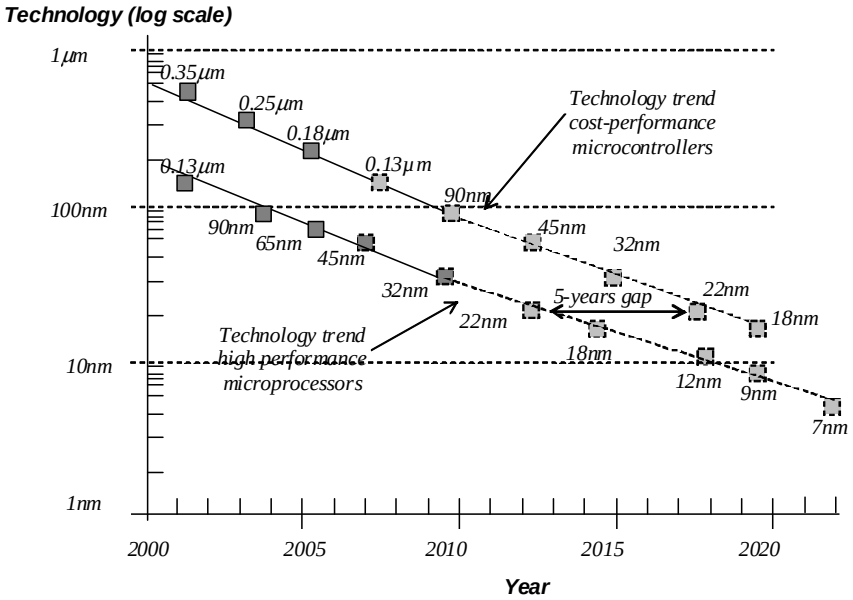

Figure 1-7 : The technology scale-down towards nanoscale devices associated with microprocessor and microcontroller manufacture [1-5]

There is a growing demand for low emission integrated circuits, especially in critical embed systems market (e.g. automotive, aerospace, medical applications…). Applying low emission design rules is required and usually efficient, but several questions rise:

⇒ Is there an optimum value and placement for the on-chip decoupling capacitance?
⇒ Is the floor planning optimum regarding low parasitic emission?
⇒ To which extend would the block placement inside the IC affect the EMI?
⇒ Would technological options such as bulk isolation reduce the emission?

Answering to such questions requires accurate EMI models, adequate simulation tools and a reliable EMI prediction methodology.

1.3 Susceptibility of integrated circuits

1.3.1 Basic mechanisms of susceptibility to radiofrequency interferences

Susceptibility to electromagnetic noise has played a significant role in the design of integrated circuits for many years and remains a major concern with the multiplication of powerful parasitic sources which can affect circuit behavior, such as mobile phones, high speed networks and wireless systems (Fig. 1-8) [1-6].

Either by common impedance, radiated coupling, mutual coupling or capacitive coupling, the disturbances can couple and propagate toward the possible entry points of the integrated circuit: inputs, outputs, peripheral and core supply or via the common substrate. Disturbances can cause temporary malfunctions (as binary errors, voltage drifts, jitter, unwanted resets…) or even permanent damages of the electronic equipment (oxide breakdown, latch-up…). In automotive applications, most of the internal disturbances are generated during the normal operation of the vehicle by sources like the ignition system, the generator and alternator system, the switching of electric motors or the actuators.

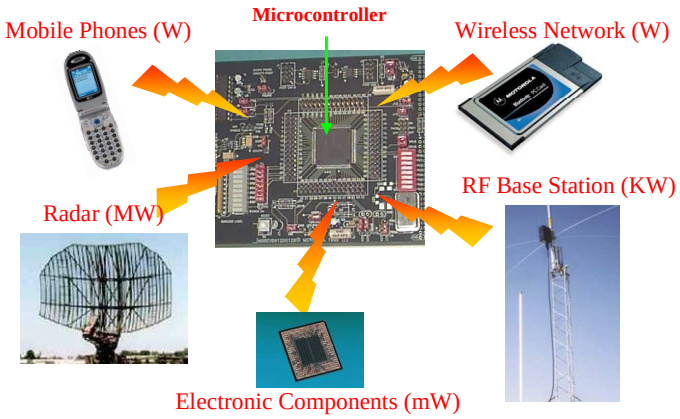

Figure 1-8 : Parasitic radio-frequency sources which may disturb integrated circuits

Susceptibility of circuits is strongly dependent on the disturbed block type and circuit design. However, some general parameters which can directly influence the susceptibility can be listed (table 1-4). The knowledge of these influent parameters helps to clarify susceptibility origins and propose immunity improvement techniques. Digital noise margins are related to technology and power supply voltage. Analog circuits often present higher susceptibility levels than digital circuit, due to smaller noise margin. Table 1-5 compares the typical ranges of sensitivity to noise for several types of ICs.

Susceptibility of electronic devices is also strongly dependent of the ability to electromagnetic interferences to couple (Fig. 1-9) and is related to the disturbance frequencies. For frequency range from 3 to 30 MHz, the disturbance may couple efficiently to very large metallic structures such as airplanes or cars. The usual criterion is one quarter of the wavelength (lambda/4). From 30 to 300 MHz, the most efficient antenna effect occurs for metal connectors around 1m, while from 3 to 30 GHz, the antenna size is the order of some centimeters (Fig. 1-10). At these frequencies, any metallic conductors (from PCB tracks to package leads) can act as an antenna and collect a large amount of noise.

Influent circuit parameters	**Comments**
Susceptibility level of an IC block	Robustness of any circuits to RF disturbances is characterized by: ▪ Noise margins: it defines the highest amplitude that a circuit can withstand to ensure a nominal activity. Static and dynamic noise margins can be distinguished. Static margin concerns continuous noise, while dynamic margin concerns fast transient noise. ▪ Delay margins: it is linked to set-up and hold time constraints of digital circuits. It defines the maximum admissible delay between two signals.
Filtering effect of the circuit	Interconnections, on-chip decoupling capacitor and parasitic coupling paths have an influence on external noise within a circuit.
Non linearity issues	IC behaviour is highly non linear (transistors, diodes, clamps). Non linear structures in the presence of average amplitude RF disturbance induce signal rectifications which modify circuit operating points.
Node impedance	Impedances of circuit nodes affect the coupling of a disturbance and thus and the susceptibility.

Table 1-4: Influent circuit parameters on susceptibility

Functions	**Noise margin digital inverter**	**12 bits ADC, 2.5 V supply**	**3G front-end**
Sensitivity level	~100 mV	~ 600 µV	~10 µV

Table 1-5 : Typical sensitivity of the on-chip analog functions

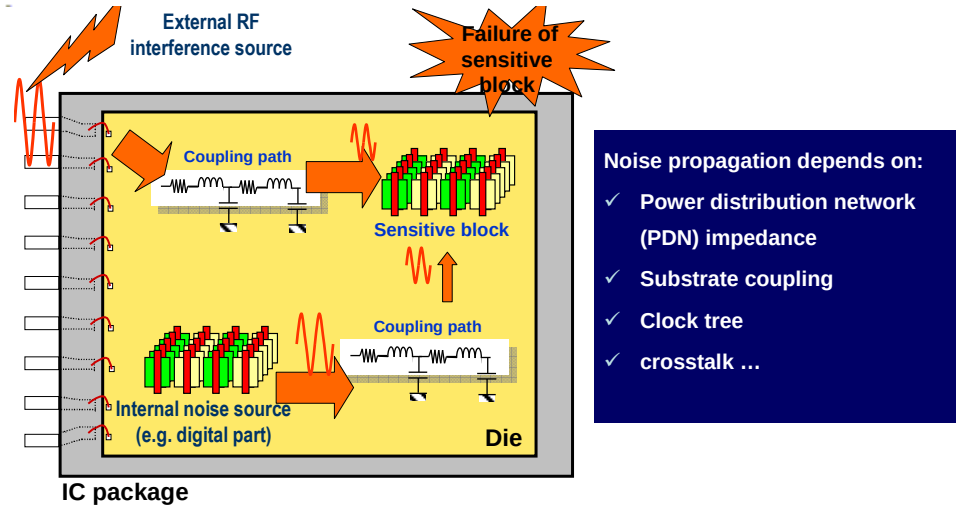

Figure 1-9 : The susceptibility of an integrated circuit depends on the coupling efficiency of an electromagnetic interference

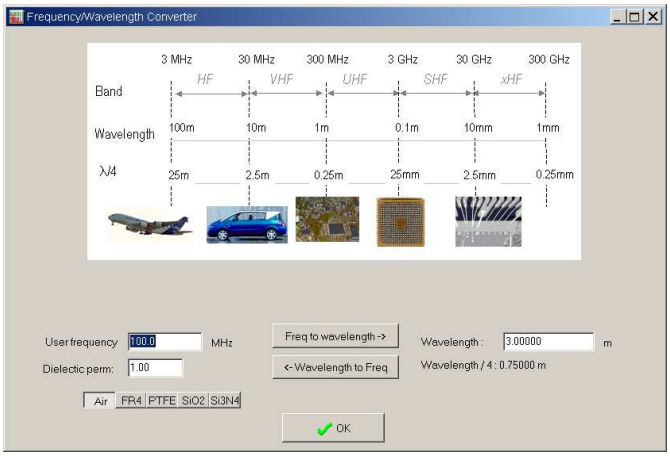

*Figure 1-10 : Link between interference frequency and antenna effect (**Tools → Freq/Wavelength converter**)*

1.3.2 Influence of IC technological evolution on susceptibility

The trend for micro-miniaturization described in table 1-2 has major consequences on integrated circuits (ICs) immunity. First, the constant supply voltage decrease reduces the static noise margin of electrical signals and thus increases the IC susceptibility to RFI. Then, as cut-off frequencies increase, circuits become sensitive to faster transient signals.

Although integrated circuits have efficient protections against transient disturbances such as electro-static discharges (ESD), the integrated circuit may withstand less and less electrical noise on power and signal pins due to a continuous decrease of voltage supply. The usual noise margin is +/- 20 % of the nominal supply voltage. In modern 65-nm CMOS process, the supply voltage of 1.0 V leads to a +/-200 mV noise margin. The noise margin should decrease to 0.1 V by 2015 according to the roadmap of Fig. 1-11. The amount of noise required to cause a malfunction can vary widely from one IC design to another.

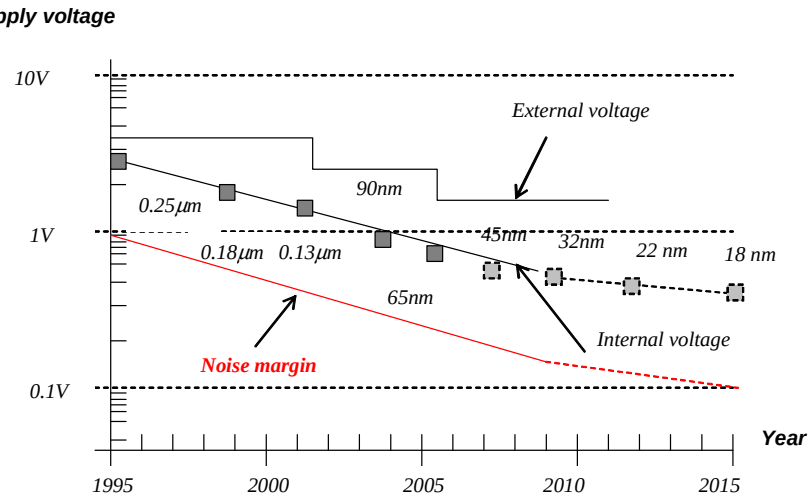

Figure 1-11 : The reduction of internal supply voltage leads to a reduced noise margin

With the newest technologies, nearly one billion devices related to mixed analogue, digital and power technologies share the same piece of silicon. Some parts of the chip generate EMI while the others have very low sensitivities regarding the EMI level. It is an issue to ensure that all the embedded functions are able to operate (auto-compatibility) [1-7].
Applying low susceptibility design rules is usually efficient, but several questions rise:

- ⇒ Is there an optimum value and placement for the on-chip decoupling capacitance?
- ⇒ Is the floor planning optimum regarding low parasitic susceptibility?
- ⇒ To which extend would the block placement inside the IC affect the susceptibility?
- ⇒ Would technological options affect the susceptibility?

Answering to such questions requires accurate EMI models, adequate simulation tools and a reliable EMI prediction methodology.

1.4 References

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1.5 Exercises

1. Exercise 1

Estimate the switching current of a 32 bit microcontroller which presents the following characteristics:

- each gate consumes 0.1 mA during 100ps
- the IC contains 1 billion gates
- only 10% of the gates switch simultaneously
- the activity is spread over 1 ns due to non-synchronous switching

2. Exercise 2

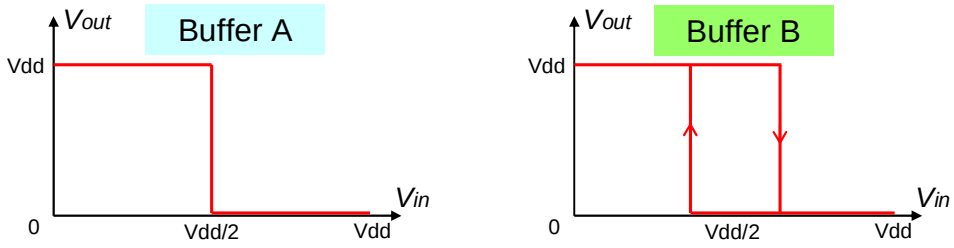
The previous circuit is mounted in a QFP package. The circuit is supplied by a single power supply pair (Vdd and Vss) associated to 2 leads of the package. For this type of package, inductance of leads can be estimated about 10 nH. Estimate the maximum power supply voltage drop. Comment the result.

3. Exercise 3

Typical constraint in term of power supply voltage ripple for digital circuit is set at 10 % of the power supply voltage. Suppose that a 10-bit analog-to-digital converter (ADC) embedded in a mixed signal circuit which shares its power supply with a digital core. What could be the consequence on the ADC conversion result?

4. Exercise 4

The following figure presents the input voltage transfer characteristics of two versions of a CMOS input buffer. Which version is the more susceptible to radiofrequency interferences?



2 Getting started with IC-EMC

IC-EMC is a simulation software entirely dedicated to the EMC of ICs issues. It works only with Windows 2000, XP, Vista and Windows 7. IC-EMC is a schematic editor interfaced with the analog simulator WinSPICE [2-1]. By exploiting simulation results provided by WinSPICE, IC-EMC proposes a set of post-processing tools to extract relevant EMC information.

2.1 Overview of the software IC-EMC

The tool IC-EMC is able to perform comparisons between measurements and simulation of conducted, radiated emission, near-field emission, impedance and immunity, as illustrated in Fig. 2-1. Moreover, it includes IC analysis tools a 3D package viewer and a near-field emission simulator.

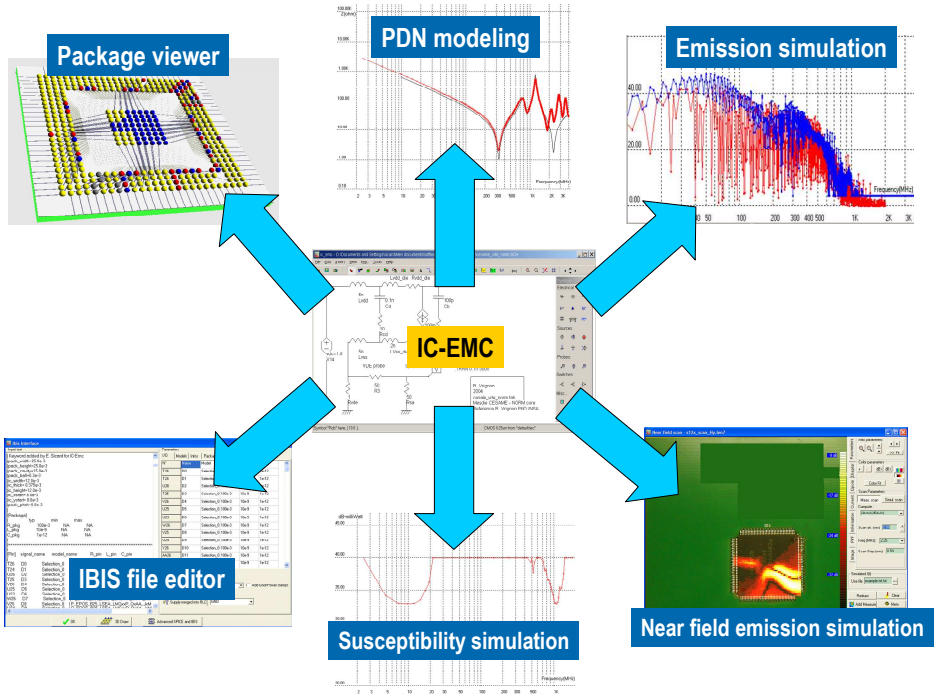


Figure 2-1 : Main features of IC-EMC

The main commands of IC-EMC are shown in figure 2-2. From left to right, the Spice Simulation icon translates the schematic diagram into a SPICE compatible text file, the next icons give access to the emission spectrum window, the impedance vs. frequency, the immunity simulation screen, and the near-field simulation screen.

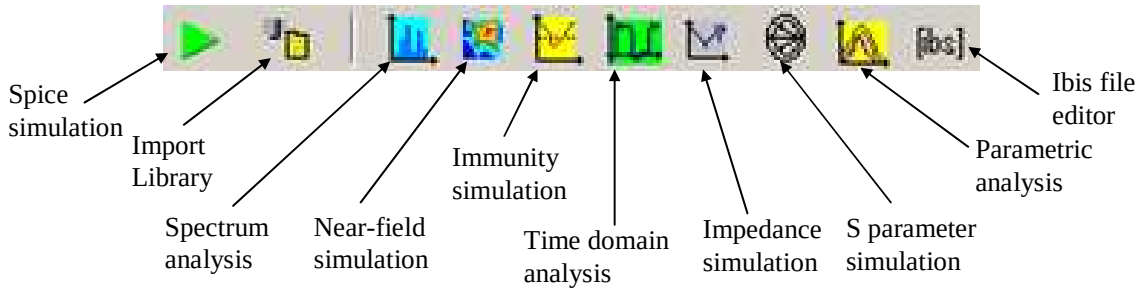


Figure 2-2 : Main commands proposed by -EMC

Figure 2-3 describes the general simulation flow with IC-EMC. The process starts with the edition of the circuit schematic. Component models are provided by IC-EMC or external libraries. The netlist file generated by IC-EMC serves as input file for WinSPICE simulator. At the end of the simulation,

WinSPICE results are exploited by IC-EMC post-processing tools. Different measurement file formats can be imported to compare simulation and measurement results and tune simulation models.

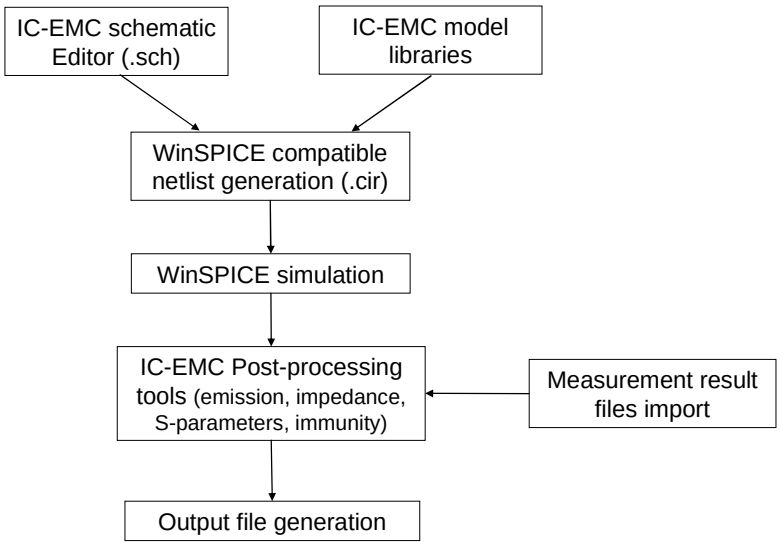


Figure 2-3 : General simulation flow with IC-EMC

2.2 Launch IC-EMC

The following paragraphs detail the different steps to install, launch and exit the software.

2.2.1 Download the Schematic Editor

The schematic editor may be downloaded from www.ic-emc.org [2-2].

⇒ Click the item "Download", and chose "IC-EMC" in the software section.
⇒ Save the ZIP file on your hard disk, preferably in a new directory, for example called "Ic-emc".
⇒ Unzip the contents of the file
⇒ In "/system" directory, double click the executable file ICEM.EXE

The system directory contains a large number of subdirectories. Their contents are described in part 2.6.

2.2.2 Dowload WinSpice

WinSPICE may be downloaded as a shareware from www.winspice.com [2-1].

2.2.3 Initial Screen

The main screen of the schematic editor is shown in figure 2-4. The editor contains a palette of symbols (Window "Symbol Library" situated on the right of the screen) and some basic editing icons to build the schematic diagram of the circuit and to control the main EMC screens.

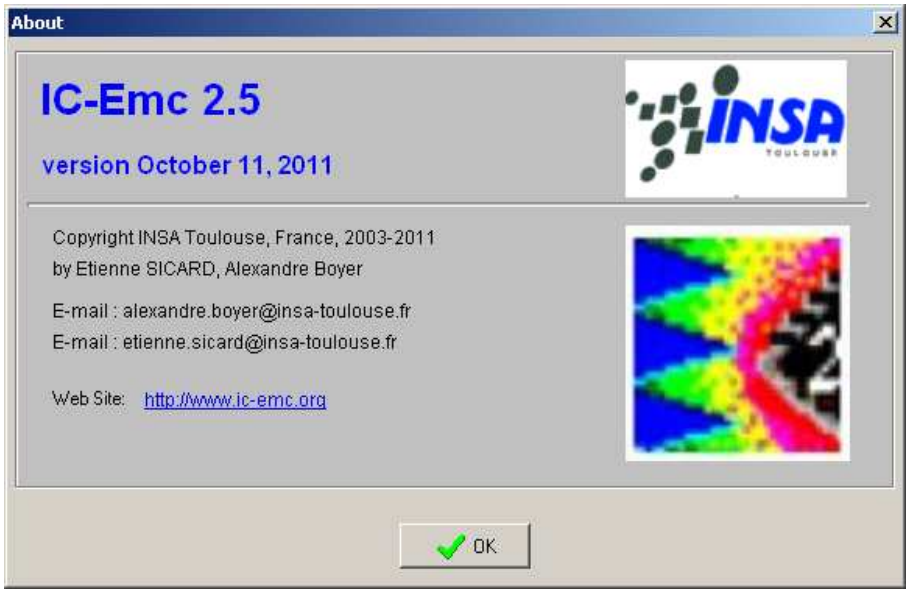


Figure 2-4: The default screen of the IC-EMC schematic editor

2.2.4 Close WinSpice

Enter the command “quit” and confirm by “yes”.

2.2.5 Close IC-EMC

Click “File → Exit IC-EMC”

2.3 Example 1: Conducted emission of a microcontroller MPC555 simulation

This first example aims at presenting the flow to simulate the conducted emission of a microcontroller, with a simplified model of a microcontroller. Simulated conducted emission measurements are related to the standard IEC 61967-4 1/150 Ω method [2-3].

2.3.1 Load the example

Load the file "getting started\mpc\mpc_vde.sch" (Fig. 2-5). A 32-bit micro-controller is described using basic RLC elements, according to ICEM model format (see chapter 5), the IBIS elements for the package (see chapter 4), and the current measurement probe dedfined by the standard IEC 61967-4 1/150 Ω method [2-3]. ICEM and IBIS models are IEC standards dedicated to emission and I/O modeling respectively. They are widely used in the different case studies provided by IC-EMC.

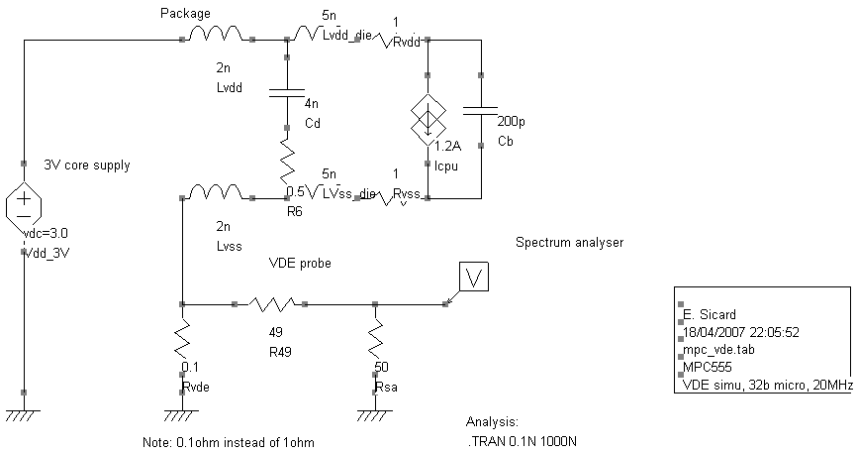


Figure 2-5: The ICEM model of a 32bit micro-controller (getting_started\mpc\mpc_vde.SCH)

Parameters	Description	Remarks
Ib	Current source. Unit: Ampere Description: piece-wise-linear	*The Ib current is described as a periodic triangle (1.2 A max)*
Cd	Decoupling capacitance. Unit: Farad Description: discrete C	*Cd is 4 nF, which is quite high due to on-chip added capacitance*
Lvdd_die, Lvss_die	Serial internal inductance. Unit: Henry Description: discrete L	*The serial inductance is tuned to 5 nH, which provokes a resonance effect with Cb around 300 MHz.*
Rvdd_die, Rvss_die	Serial internal resistance. Unit: Ohm Description: discrete R	*Around 1 ohm serial resistance due to long metal tracks on-chip*
Cb	Block decoupling capacitance. Unit: Farad Description: discrete C	*Local block capacitance, around 200 pF.*
Rvde, R49, Rsa	Current probe, matching resistors, and input impedance of spectrum analyzer respectively Unit: Ohm Description: discrete R	*Usually, the current probe resistor is equal to 1 ohm. To reduce voltage drops across this resistor, it has been replaced by 0.1 ohm.*

Table 2-1 : Details on basic electrical elements (getting_started\mpc\mpc_vde.SCH)

Elements concerning the package are *Lvdd* and *Lvss*, accounting for the serial equivalent inductance from the die of the IC to the physical supply source, and the VDE probe. Notice that the serial resistance is 0.1 Ω instead of 1 Ω (Table 2-1) as the current flowing inside the IC is very large. Placing a 1 Ω serial resistance would dissipate nearly 1 Watt and induce a voltage drop near 1 V, which is unacceptable. The voltage measured by the spectrum analyzer V_{SA} is related to the IC current I_{gnd} returning to the ground through the resistance by the following theoretical relation (if PCB and passive device parasitics are ignored).

$$V_{SA} = \frac{1}{2} R_{VDE} I_{gnd} \qquad \textit{Equ. 2-1}$$

2.3.2 Create the SPICE file

Invoke the command *File → Generate Spice file* or click <Ctrl>+<G>. The following screen appears (Fig. 2-6). A file called "mpc_vde.cir" must have been created, which contains the netlist description of the circuit. This file constitutes the input of WinSPICE.

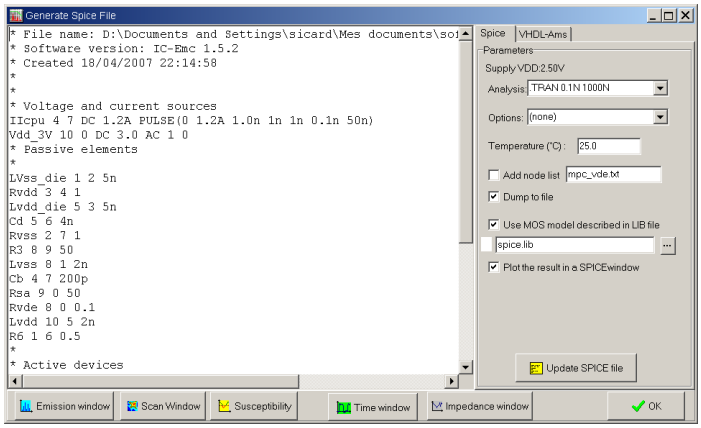


Figure 2-6: The SPICE file generated from the schematic diagram (getting_started\mpc\mpc_vde.SCH)

2.3.3 Current Source Description

Internal activity of circuit corresponds to charge/discharge cycles which can be modeled by one or several current sources, the most basic description is done by a pulse waveform. This modeling approach has been adopted by the standard ICEM, as described in chapter 5. A time-dependent value

is assigned to the current source for transient analysis. There are five independent source functions: pulse, exponential, sinusoidal, piece-wise linear and single-frequency FM. In the schematic editor, the PULSE description has been implemented, as shown in figure 2-7. The PULSE description restricts the *Ib* shape to a periodic pulse, which has a triangular shape if the pulse width parameter is set to zero.

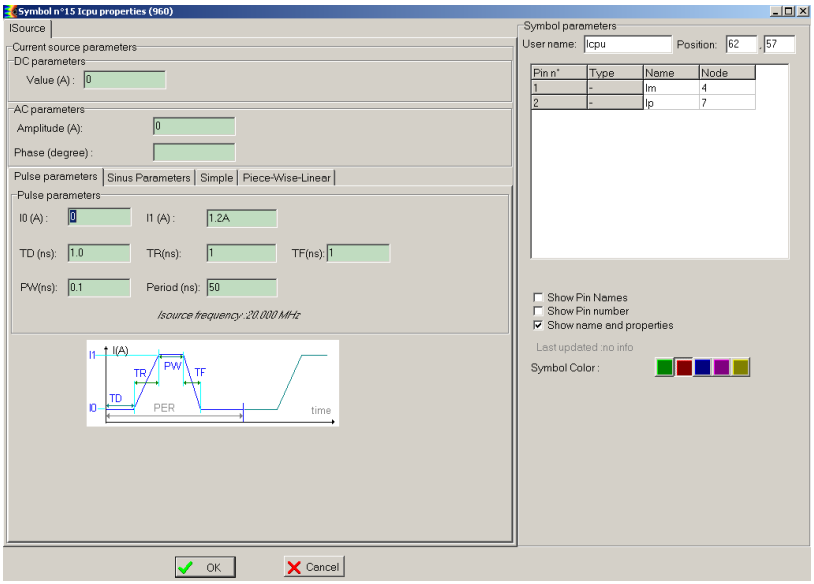


Figure 2-7: Current Pulse parameters in the schematic editor (mpc_vde.SCH)

```
PULSE(I0 I1 TD TR TF PW PER)
Example: IIcpu 5 7 PULSE(0 1.2A 1.0n 1n 1n 0.5n 50n)
```

Parameter	Description	Unit
I1	pulsed value	Amps
TD	rise time	TSTEP seconds
TF	fall time	TSTEP seconds
PW	pulse width	TSTOP seconds
PER	period	TSTOP seconds

Table 2-2 : Current source description under SPICE

2.3.4 Power supply Description

The power supply is modeled by a constant voltage source. In figure 2-8, the voltage source is constant, with a DC value of 3.0 V.

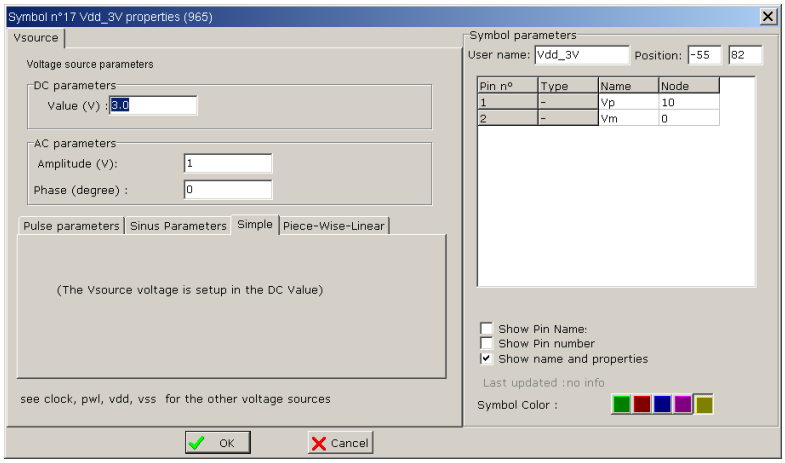


Figure 2-8 : Constant voltage source (getting_started\mpc\mpc_vde.SCH)

2.3.5 Analysis Description

In the editing window, a text is added which sets up the desired analysis. The text must start by '.TRAN' (Transient analysis), '.AC' (Small signal frequency analysis), or '.DC' (static characteristics). Chapter 11.1.47 gives more details of the text commands and associated analysis. In figure 2-9, the time-domain analysis is set to 1000 ns, with a simulation step of 0.1 ns.

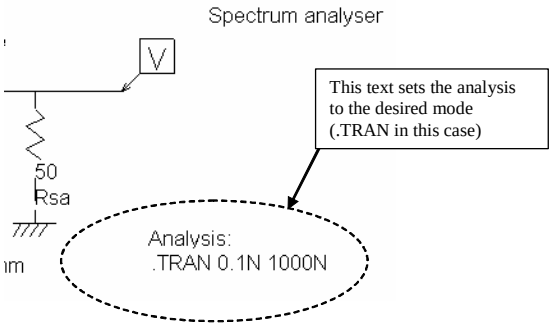


Figure 2-9 : Defining the SPICE simulation parameters

2.3.6 Run SPICE Simulation

Start the WinSpice program (here we use version 1.05.01, Dec 2003), and click "File" → "Open" (Fig. 2-10). Select the desired .CIR file. We must open the file generated by IC-EMC at the previous step that is "getting_started\mpc\ mpc_vde.CIR". The simulation is performed in time domain, and the following screen appears. The .TRAN analysis is conducted during 1000 NS. The result is stored in a file called “mpc_vde.txt”. The plot of the transient simulation appears in a new window reported in figure 2-10 right.

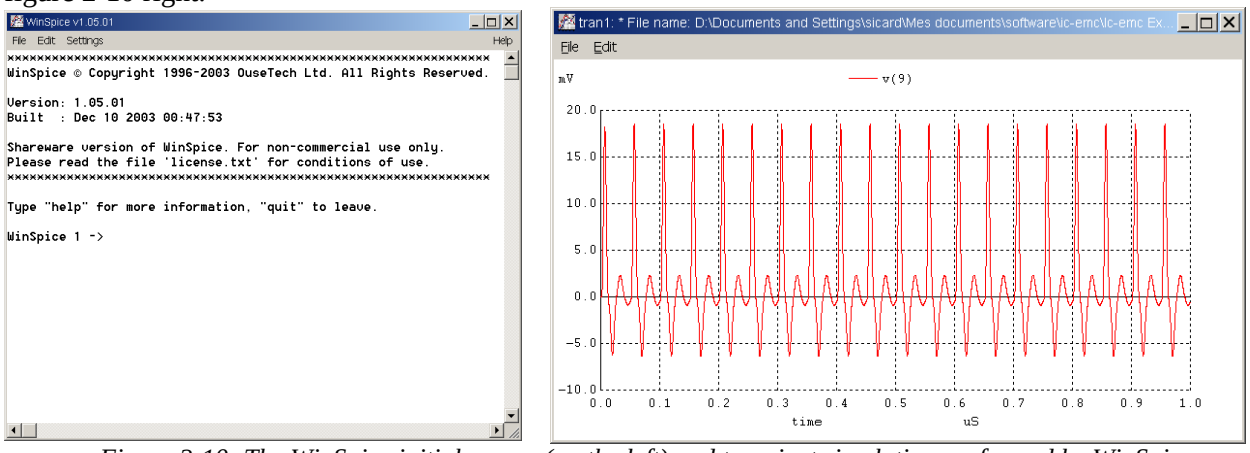


Figure 2-10: The WinSpice initial screen (on the left) and transient simulation performed by WinSpice (on the right)

2.3.7 Emission simulation

The voltage waveform computed by the analog simulator is translated into frequency domain by means of a Fast Fourier Transform (FFT). The X axis should cover the range 1-5000 MHz in logarithmic scale. The energy in Y axis is in dBµV (see section 2 for more information).

In the SPICE generator menu, click "Emission Window", or click "EMC" → "Emission dBµV vs. Frequency". Alternatively, you may click the icon above. A specific screen with Log/Log units configured to display energy vs. frequency is proposed, as shown in figure 2-11.

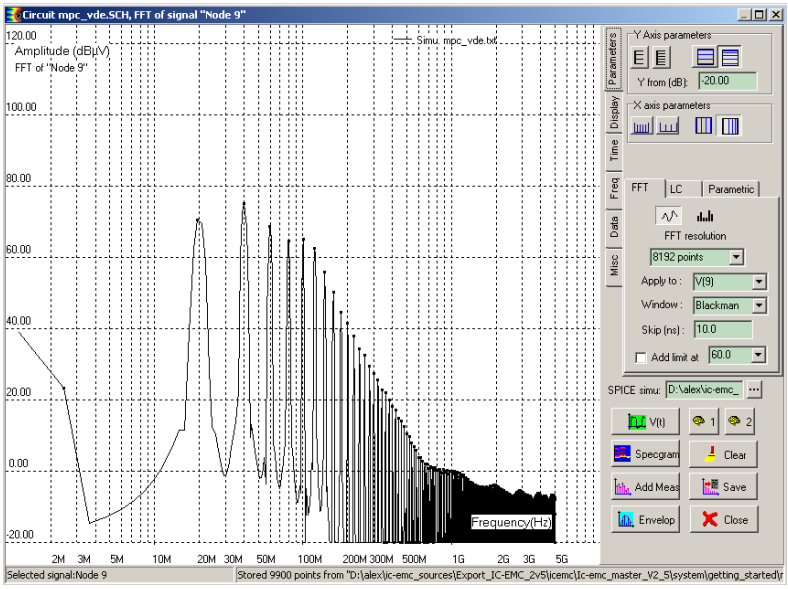


Figure 2-11: Simulation of the conducted emission of the MPC (mpc_vde.SCH)

In case the result does not appear, click the button [...] situated at the right side of "SPICE simu" and select the file "mpc_vde.txt". The spectrum appears as shown in the figure. The FFT points are adapted to fit the information included in the simulation.

2.3.8 Comparison with Measurements

In the EMC window, click "Add Measurements" to display the measurements superimposed to the simulations, for comparison purpose. An example of comparison with the measurements using the VDE 1/150 Ω method (file "mpc_vde.tab") is proposed in figure 2-12. The simulation fits with the measurement up to 260 MHz, except at 120 MHz where simulation is 10 dB above the measurement. Despite the discrepancy at this frequency, an acceptable correlation is obtained with a very simple model. Correlation with measurement can be improved, especially at high frequency, by modifying the current profile, the IC internal power supply network and board models.

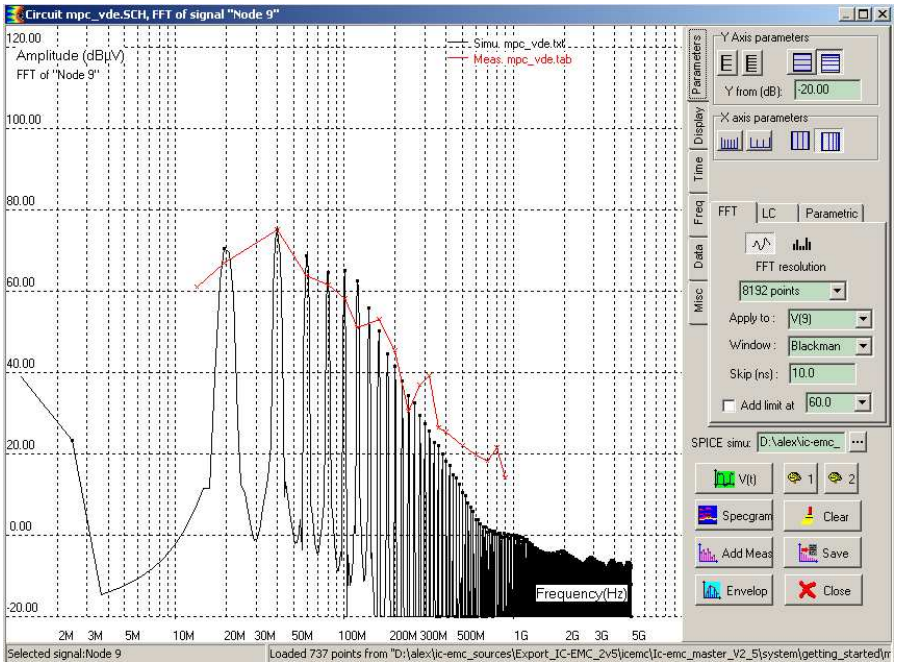


Figure 2-12 : Comparison between measured and conducted emission for a MPC microcontroller (mpc_vde.sch, mpe_vde.tab)

2.4 Example 2: Impedance analysis of the power supply network of a circuit mounted in a 64 BGA package

This second example aims at presenting the flow to simulate the impedance versus frequency of the passive decoupling network (PDN) of a small 90 nm circuit mounted in a 64 ball grid array (BGA) package. The PDN is a macroscopic block defined by ICEM standard to describe the passive network which exists between several IC accesses. Usually, the PDN of a circuit models the power supply network. The accuracy of the PDN model is fundamental for emission and susceptibility predictions as it influences directly the noise propagation within the circuit. PDN modeling can be done not only by impedance measurement, but also by S parameter measurement. Both analyses are provided by IC-EMC and will be describe in chapter 3.

2.4.1 Load the example

Load the file called "getting_started / FFIO90 / FFIO_90nm_Z_VDDE .sch" which corresponds to figure 2-13. The schematic models the PDN of a small test chip fabricated in CMOS 90 nm containing several I/O structures [2-4]. The circuit is mounted in a 64-pin BGA package, as described in figure 2-14.

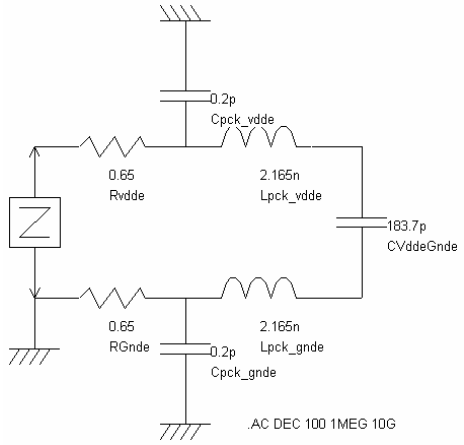


Figure 2-13: PDN model of a test chip fabricated in CMOS 90 nm containing I/O structures (getting_ started / FFIO90 / FFIO_90nm_Z_VDDE.SCH)

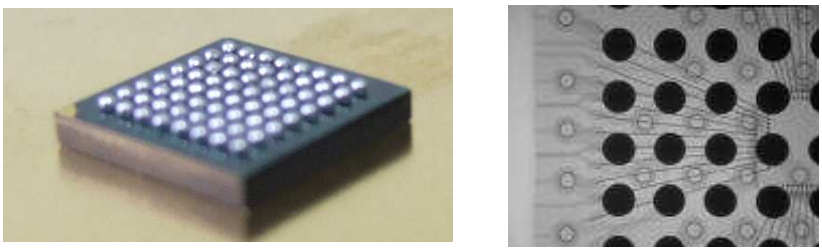


Figure 2-14: 64-pin LBGA package [2-4]

Measurements have been performed using a Vector Network Analyzer (VNA) directly on the package balls with a coplanar probe placed between adjacent power pins VDDE and GNDE. The model has been extracted from the [s] measurements (see chapter 3.9). The PDN model includes two parts:

- the die contribution, i.e. interconnections and on-chip decoupling capacitances
- the package contribution, i.e inductive effects of balls, vias and bonding wires constituting the BGA package

Table 2-3 gives details of the elements of the model.

Parameters	Description	Remarks
CVddeGnde	Equivalent on-chip capacitance Unit: Farad Description: discrete capacitance	This element models all parasitic and intentional on-chip capacitances between power supply VDDE and ground GNDE access.
Lpck_vdde, Lpck_gnde	Package parasitic inductance Unit: Henry Description: discrete inductance	These 2 inductances model the contribution of all elements of VDDE and GNDE pins. With on-chip capacitance, they are responsible of the first resonance.
Cpck_vdde, Cpck_gnde	Package parasitic capacitance Unit: Farad Description: discrete capacitance	These 2 capacitances model the contribution of all elements of VDDE and GNDE pins. They are added to model the package self resonance which appears above several GHz.
RVdde, RGnde	Total power supply and ground resistance Unit: Ohm Description: discrete resistance	These resistors represent the resistive contribution of package and on-chip interconnections. Their effect is negligible except at resonance frequency.

Table 2-3 : Details of basic elements of FFIO_90nm_Z_VDDE.sch

2.4.2 Impedance probe description

The impedance analysis corresponds to a simulation of the input impedance (also written Zin or Z11) seen from one circuit access relatively to a reference. In this example, the access is the power supply pin VDDE. Measurement is referenced to the ground pin GNDE.
Impedance simulation is allowed only if an impedance probe or Z probe is placed in the schematic diagram. The Z probe (Fig. 2-15) is accessible from the palette. If we double click on the Z probe, the property screen is displayed, but without any specific property. However, the Z probe is not a transparent symbol and it creates a voltage source in the netlist as described below:

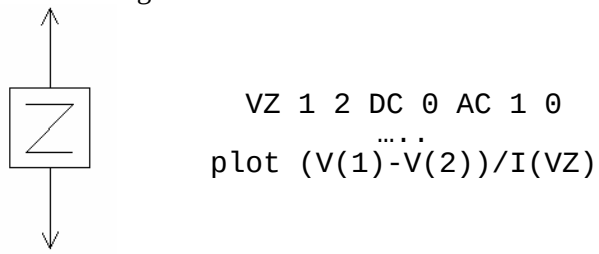


Figure 2-15: Impedance probe and associated SPICE description

The voltage source associated to the Z probe is an AC source with amplitude of 1 V. As may be found at the end of the SPICE netlist, a “plot” control is associated with an equation which computes the impedance by dividing the voltage amplitude across the probe by the current provided by the impedance probe.

Remark: use only one impedance probe per schematic diagram. The input impedance is linked to the current that a perfect voltage source delivers to a circuit. If a second AC voltage source is present, it will modify the current which flows along the branch of the first Z probe and hence the input impedance.

2.4.3 Analysis description

Impedance simulation is a small signal frequency analysis, so that it requires an AC simulation. In the editing window, a text is added which sets up the desired analysis. The text must start by ‘.AC’ followed by the AC simulation parameters (see 11.1.44 for more details on simulation commands). In figure 2-14, the frequency sampling is logarithmic; 100 points per decade are required between 1 MHz and 10 GHz.

2.4.4 Run SPICE simulation

Start the WinSpice program (here we use version 1.05.01, Dec 2003), and click "File" → "Open". Select the desired .CIR file. We must open the file generated by IC-EMC at the previous step that is "FFIO_90nm_Z_VDDE.CIR". The simulation is performed in frequency domain and the following screen appears.

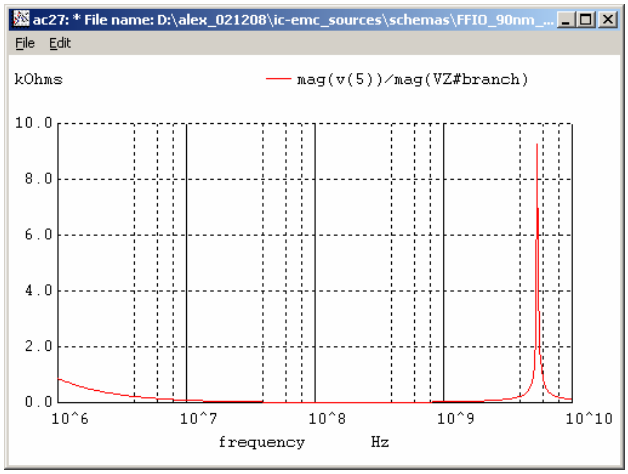


Figure 2-16: AC simulation performed by WinSPICE (FFIO_90nm_Z_VDDE.txt)

2.4.5 Impedance analysis

The impedance profile vs. frequency computed by WinSPICE can be displayed in a specific screen dedicated to impedance analysis. In the SPICE generator menu, click "Impedance Window", or click "EMC" → "Impedance vs. Frequency". Alternatively, you may click the icon  . A specific screen with Log/Log units configured to display impedance vs. frequency is proposed, as shown in figure 2-17. At low frequency, impedance tends to decrease due to the on-chip capacitance effect. At 180 MHz, the first resonance linked to the on-chip capacitance and the package inductances appears. A second resonance due to package inductance and capacitance appears at 5.4 GHz.

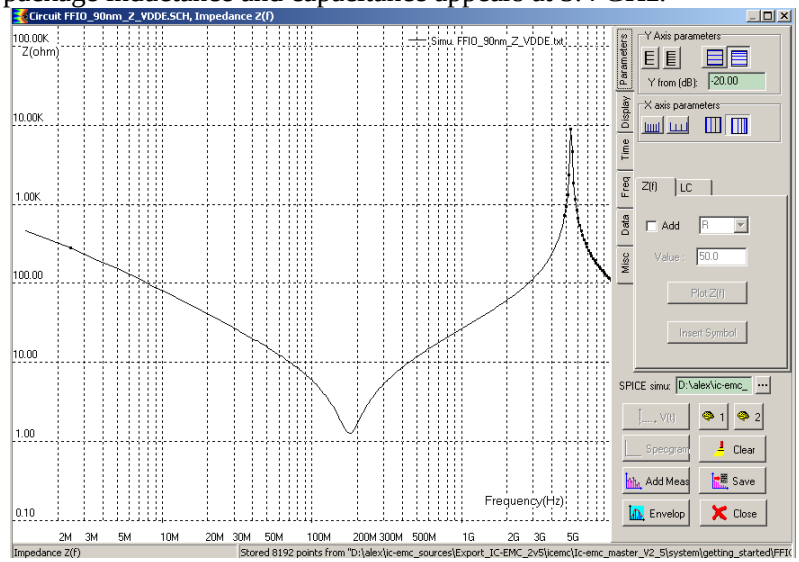


Figure 2-17: Input impedance simulation performed by WinSPICE (getting started / FFIO90 / FFIO_90nm_Z_VDDE.sch)

2.4.6 Comparison with measurement

In the impedance window, click “Add Meas” to display the impedance measurement of the PDN of the circuit. The measurement data are available in the file called “Z11_FFIO_VDDE_A4B5.z”. The comparison between measurement and simulation is presented in figure 2-18 and proves the validity of the model up to 3 GHz.

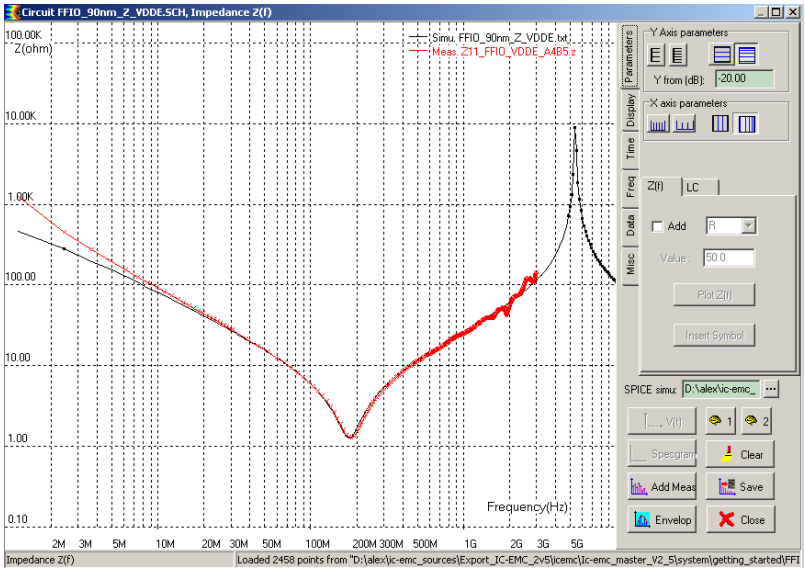


Figure 2-18: Comparison between measured and simulated input impedance of the PDN of the 90 nm circuit (Z11_FFIO_VDDE_A4B5.z)

2.5 Example 3: Simulation of the conducted immunity on the power supply of a microcontroller

This third example aims at presenting the flow to simulate the susceptibility of a circuit to radiofrequency interference (RFI). In this short case study, a sinusoidal conducted disturbance is injected on the power supply network of a digital circuit until the noise level measured on the pin of an output buffer exceeds the noise margin. The circuit under test is a S12X microcontroller described in chapter 8 (S12X Case Study). Conducted emission measurements are related to the standard IEC 62132-3 Direct Power Injection (DPI) method [2-5] and are performed from 1 MHz up to 1000 MHz. First, a basic passive model of the power distribution network (PDN) of the circuit under test is extracted from [s] parameter measurement. The same PDN is reused for the susceptibility prediction. The following sections describe the different steps used to build the susceptibility model and to simulate the susceptibility vs. frequency of the microcontroller.

2.5.1 Load the S parameter simulation model

Load the file called “getting started\S12X_RFI\S12XPowerSupply_S11.sch”, as described in figure 2-19. The proposed model is dedicated to a [s] parameter simulation for validating the passive model of the circuit under test. The model has been extracted by a vector network analyzer measurement from 300 KHz up to 3 GHz, which has been performed through a SMA connector on the power supply plane.

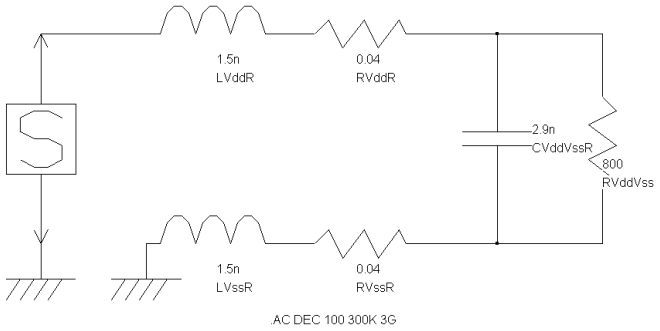


Figure 2-19: Basic PDN model of the S12X microcontroller (getting_ started \S12X_RFI \S12XPowerSupply_S11.sch)

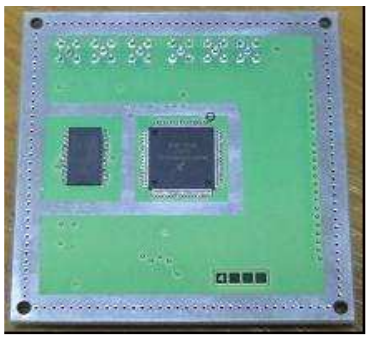


Figure 2-20: EMC board of the S12X microcontroller

Parameters	Description	Remarks
LVddR, LVssR	Package and board parasitic inductance Unit: Henry Description: discrete inductance	These 2 inductances model the contribution of all the Vdd and Vss pins of the S12X package and the parasitic inductance of power supply and ground planes of the board
RVddR, RVssR	Package and board parasitic resistance Unit: Ohm Description: discrete resistance	These resistors represent the resistive contribution of all the elements between Vdd and Vss (board, package, die).
CVddVssR	Circuit and board capacitance Unit: Farad Description: discrete capacitance	This capacitance models the total capacitance between Vdd and Vss. It is the sum of board interplane capacitance and all the on-chip capacitances between Vdd and Vss
RVddVssR	Loss resistance Unit: Ohm Description: discrete resistance	This resistance is added between Vdd and Vss and models all the dielectric losses between power and ground plane and on-chip leakage between Vdd and Vss

Table 2-4 : Details of basic elements of S12XPowerSupply_S11.sch

The S12X microcontroller is mounted on a specific board dedicated to EMC board (Fig. 2-20). The circuit is supplied through five power supply pairs, which are connected to common internal power supply and ground planes. Table 2-4 gives details of the elements of the PDN model.

2.5.2 [s] parameter port probe

A [s] parameter port probe is inserted in a schematic to perform a [s] parameter simulation between N ports. [s] parameters are used to characterize reflection and transfer function between each port of a device under test (cf. section 3.9 “[s] parameters”).
[s] parameter simulation is allowed only if [s] parameter port probe or [s] probe is placed within the schematic. The [s] probe is accessible from the palette . If you double click on the [s] probe, the property screen is displayed (Fig. 2-21). A port is characterized by a unique number, a characteristic impedance *Zc* (common to every port) and a DC voltage. A port can be disabled so that it is replaced by a resistance with a value of *Zc*. This probe allows a simulation of the reflection coefficient seen from this port.

Figure 2-21: S parameter port probe properties

2.5.3 [s] parameter analysis description

The [s] parameter simulation is based on a small signal frequency analysis (AC simulation). This analysis is also referred as small signal [s] parameter analysis in common simulator. In the editing window, a text is added which sets up the desired analysis. The text must start by '.AC' followed by the AC simulation parameters (see 11.1.47 for more details on simulation commands). In figure 2-19, the frequency sampling is logarithmic, with 100 points per decade between 300 KHz and 3 GHz.

2.5.4 Run SPICE simulation

Start the WinSpice program (here we use version 1.05.01, Dec 2003), and click "File" → "Open". Select the desired .CIR file. We must open the file generated by IC-EMC at the previous step that is "S12XPowerSupply_S11.CIR". If a schematic contains N ports, the simulation will be repeated N^2 times in order to characterize all the couplings between the different ports. The status of each simulation is displayed on WinSPICE interface (fig. 2-22). The simulation is performed in frequency domain and the following screen appears. The unit of the Y axis has no unit (a [s] parameter is a ratio between two voltages).

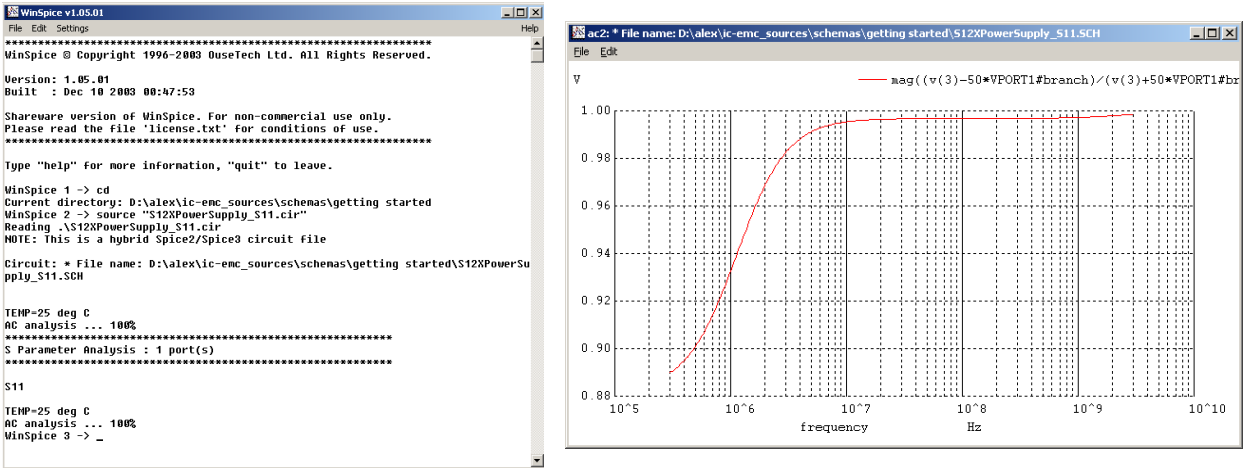


Figure 2-22: S parameter simulation performed by WinSPICE (getting started\S12X_RFI\S12XPowerSupply_S11.cir)

2.5.5 S parameter analysis and comparison with measurements

Click "Impedance Window", or click "EMC" → "S parameters" to open the [s] parameter display screen. Alternatively, you may click the icon  . A specific screen with a blank screen and a menu on the right appears. In the menu, check that "S parameter" box is set at "S11" and "Format" at "Mag (linear)" and click on the button Add to display the amplitude of the simulated reflection coefficient, as shown on figure 2-23. Check the box "Log" under "X axis" to have a logarithmic frequency axis.

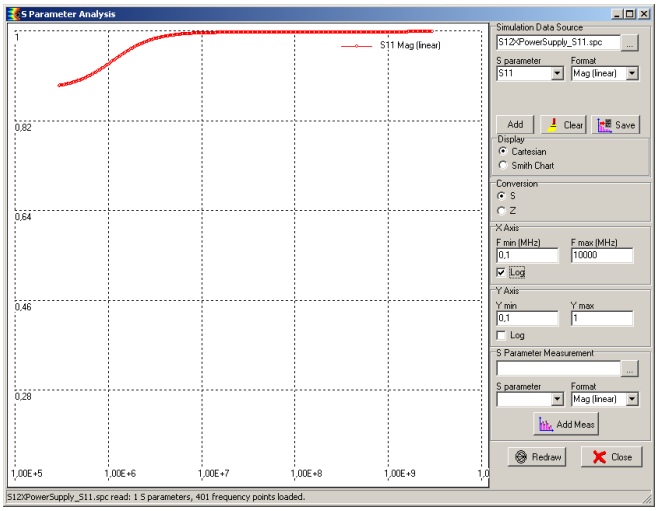


Figure 2-23: Simulation of the amplitude of S11 parameter (getting_started \S12X_RFI \S12XPowerSupply_S11.sch)

S11 measurements are included in the file “S12XPowerSupply_S11Meas.s1p”. This file is in the Touchstone standard format (see section 12.5). Select this file in the field “S parameter measurement”, choose the adequate format with the fields “S parameter” and “Format” and finally click on the button “Add Meas” to display the measurement on screen. Figure 2-25 presents the comparison between measurement and simulation of the amplitude of the S11 parameter (Y axis have been modified) and shows a good agreement between 1 and 100 MHz.
The format of the parameter can be modified. For example, the phase of the simulated and measured can be displayed. Click on the button “Clear”, select “Phase (degree)” in the field formats and click on the buttons “Add” and “Add Meas”. Figure 2-24 shows the comparison between the measured and simulated phase of the reflection coefficient and confirm the good correlation between measurement and simulation up to 100 MHz.

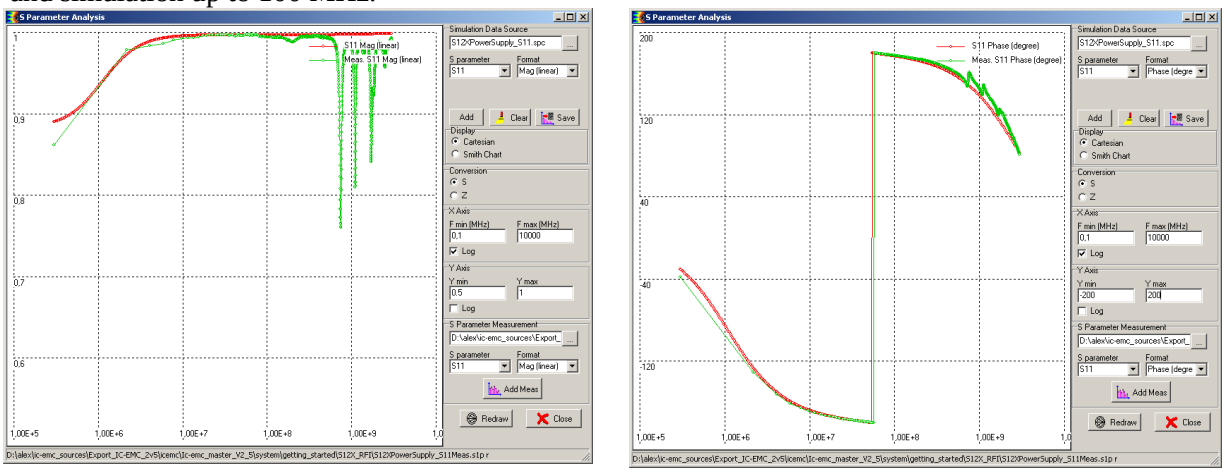


Figure 2-24: Comparison between measured and simulated amplitude (on the left) and phase (on the right) of the S11 parameter (S12XPowerSupply_S11.sch)

2.5.6 Load the susceptibility simulation model

A basic susceptibility to RFI model is built from the extracted PDN. Load the file “RFI_S12XPowerSupply.sch” described in figure 2-25. This schematic models the conducted injection of RFI in the power plane of the S12X board according to the IEC 62132-3 DPI standard [2-5]. The susceptibility of the circuit is evaluated in term of noise measured on the pin of an output buffer of the microcontroller with an oscilloscope. The output buffer is tight to a 5 V voltage. The susceptibility criterion in this test is reached when the amplitude of noise measured with the oscilloscope exceeds 1 V (20 % of the supply voltage).

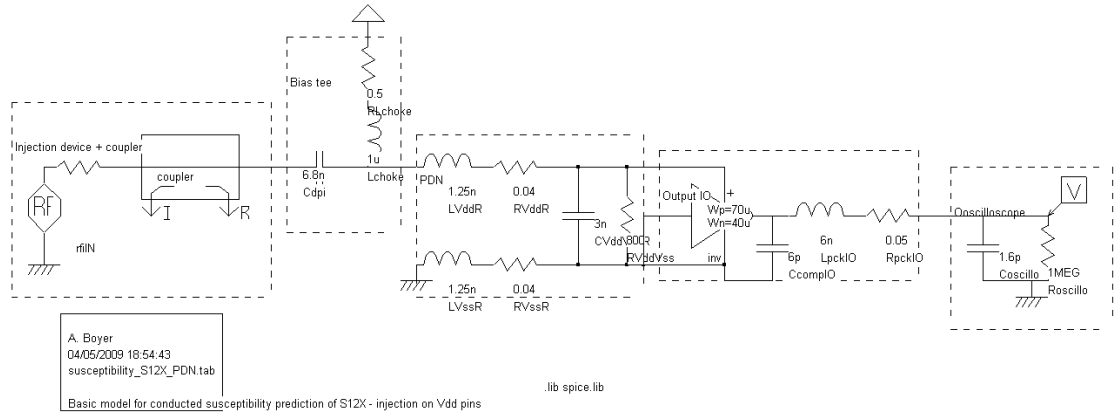


Figure 2-25: Basic model for conducted susceptibility prediction of the S12X microcontroller (getting started\S12X_RFI\RFI_S12XPowerSupply.sch)

Several new elements have been added, which are detailed in table 2-5.

Elements	Description
Injection device and coupler	The injection device is used to produce the RF disturbance and consists in a sinusoidal source with a 50 ohms output resistor. Frequency and amplitude of the RF disturbance varies during simulation and are controlled by user defined parameters. A coupler is added in the model to measure the forward power required to induce a failure. See chapter 7 for more information about susceptibility simulation.
Bias tee	This element composed of an injection capacitor and a choke inductance is required to superimpose a RF disturbance to a low frequency signal (e.g. the power supply voltage).
Power decoupling network (PDN)	A simple PDN model has been extracted from S parameter measurement.
Output IO	A simplified model of an output buffer has been built from the IBIS file of S12X (see chapter 4 for more information on IBIS file and chapter 8 for more details on S12X models). The model contains only the output buffer. Effects of clamp diodes, pad, package and tracks have been removed to simplify the model.
Oscilloscope	A large band oscilloscope is used to detect a failure during the susceptibility test. The output buffer is sensed by an active probe modeled by a parallel RC. The simulated susceptibility criterion is the voltage across this probe.

Table 2-5: Details of basic elements of RFI_S12XPowerSupply.sch

2.5.7 Configure the susceptibility simulation

A RFI source is inserted in the schematic to perform a susceptibility simulation. It consists in evaluating the required forward power produced by a RFI source to induce a predefined failure at different frequencies. A transient simulation is used to extract the forward power for a sinusoidal RFI disturbance at a fixed frequency. The amplitude of the RFI voltage is increased linearly during all the simulation, a post-processing is required to detect if a failure appears during the simulation and extract the forward power. The transient simulation is repeated for each frequency of the test. (See chapter 7 for more information on susceptibility tests and simulation).

The first step is the configuration of the susceptibility simulation. In the menu, click on "EMC → Susceptibility dBm vs. frequency" or on the icon  . The screen described in figure 2-26 and a time window appears. Two simulation modes are proposed:

- a manual mode, where frequency sweep is user-defined. The user simulates the circuit response at one particular frequency, gets the power corresponding to a failure criterion, and then changes the RFI frequency.
- an automatic mode, where the frequency sweep is controlled by the software. In this mode, the user configures the RFI frequency and the amplitude ranges, and extracts the susceptibility thresholds for the different frequencies at the end of the simulation.

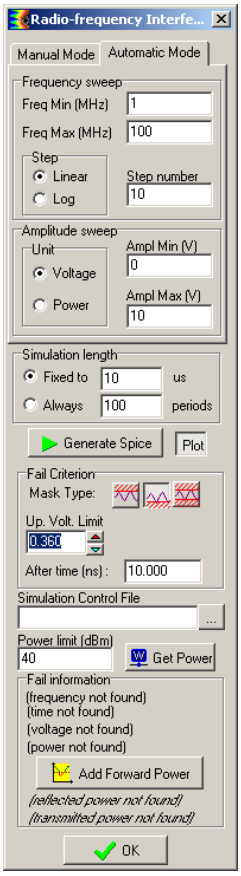


Figure 2-26: Configuration of the simulation of susceptibility

In this case study, only the automatic mode is considered. Start with the configuration of the frequency sweep: 20 points between 7 MHz and 100 MHz. Then configure the amplitude sweep, given in term of

power. The minimum power is set to 15 dBm while the maximum power is set to 45 dBm. The smaller the amplitude sweep range, the better is the accuracy of the simulation result. This value is a little higher than the injection limit of 45 dB used in measurement. Finally, configure the duration of simulation. Set it to 10 µs for every frequency. The longer the simulation time, the better is the accuracy of the simulation result. Click on the button “Generate SPICE” to create the SPICE netlist.

2.5.8 Run SPICE simulation

Start the WinSpice program (here we use version 1.05.01, Dec 2003), and click "File" → "Open". Select the desired .CIR file. We must open the file generated by IC-EMC at the previous step that is “RFI_S12XPowerSupply.CIR". As the susceptibility simulation is configured for 20 frequency points, the transient simulation is repeated 20 times. The status of each simulation is displayed on WinSPICE interface (fig. 2-27). To avoid that too many WinSPICE results open, no result windows are opened at the end of each simulation.

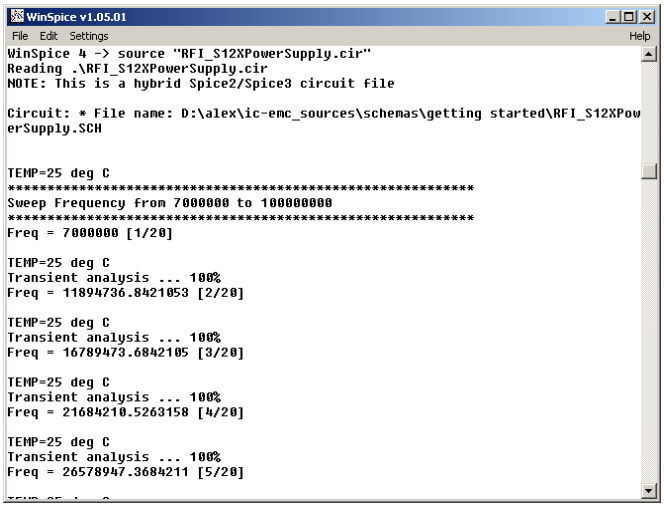


Figure 2-27: Susceptibility simulation performed by WinSPICE and frequency sweep

2.5.9 Susceptibility threshold extraction and comparison with measurement

Return to IC-EMC susceptibility simulation interface or click on “EMC → Susceptibility dBm vs. frequency” or on the icon  again. To find all the files associated to transient simulation, a simulation control file *.ctl registers all the result files. If this file does not appear in the field “Simulation control file”, select the file “RFIcontrol_RFI_S12XPowerSupply.ctl”. Then, the susceptibility criterion must be set. The nominal output signal is 5 V and the noise must remain inferior to 1 V, so that the susceptibility criterion can be detected when the output signal amplitude passes under 4 V. In the field “Fail Criterion”, type “4” and click on the button  . Set also the maximum injected power to 45 dBm in the field “Power limit (dBm)” for the frequency where a failure is not reached during simulation. Finally, click on the button “Get power”.

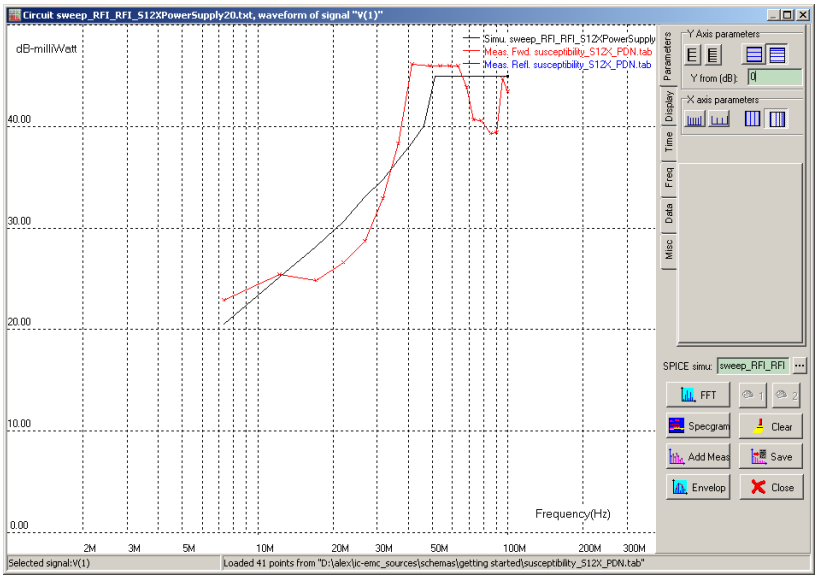


Figure 2-28: Comparison between measurement and simulation of the susceptibility threshold of the S12X microcontroller (getting started\S12X_RFI\RFI_S12XPowerSupply.sch)

On the time domain window, the waveform of the output signal is plotted and the forward power is extracted at each frequency of the simulation. At the end of this extraction, click on the button "Add Forward Power" to plot the susceptibility threshold on a Power vs. Frequency graph, as shown in figure 2-28. Click on the button "Add Meas" and select the file "susceptibility_S12X_PDN.tab" to display the measured susceptibility threshold. Figure 2-28 presents the comparison between measurement and simulation. Despite the gap that can reach up to 6 dB, simulated and measured thresholds follow the same trend and have the same order so that the susceptibility level of the circuit can be easily and quickly estimated on a large range of frequency. Increasing the complexity of board and circuit models could improve the accuracy of the simulation.

2.6 Description of IC-EMC directories organization

After downloading and unzipping IC-EMC software package, a directory called "Ic-emc_master_V2_5" appears. This directory contains a directory called "system"", organized as shown in figure 2-29.
It contains the executable IC-EMC and a collection of subdirectories. Some of them contain examples, case studies other contains component libraries. Their content is briefly described in table 2-6.

Figure 2-29: Organization of the directory Ic-emc_master_V2_5/system

Subdirectory name	Content
ieee	Symbol library used by IC-EMC (*.sym). Some are available from the palette (see 11.2.7), other can be loaded by clicking on “Insert → User Symbol (.SYM)”.
html	HTML pages of online help
lib	.tec file and default non linear device SPICE library (.lib) (diode, transistor, non linear capacitor)
EMC_lib	Schematics of various EMC devices and test benches (BCI, 1/150 ohm, TEM cell…), and several examples of passive device models.
package	Geometrical models (*.geo) of various type of IC package, for extraction of electrical parasitics
passive	Schematic of various passive devices (resistor, capacitor, inductor, ferrite)
Getting_started	Schematics and measurements presented in chapter 2 – Getting started
basic	Schematics presented in chapter 3 – Basic concepts
ibis	Schematics and IBIS file presented in chapter 4 – IBIS standard
emission	Schematics and measurements presented in chapter 5 – Emission simulation
Near_field	Schematics and measurements presented in chapter 6 – Near field scanning
immunity	Schematics and measurements presented in chapter 7 – Immunity simulation
Case_study	Several real case studies, some of them are described in chapter 8 – Case studies.

Table 2-6: Content of the subdirectories of Ic-emc_master_V2_5\system

2.7 Summary

This chapter provided a first introduction of the software IC-EMC with the main commands and the general simulation flow. Basic procedures to launch IC-EMC and the analog simulator WinSPICE were described. Three simple basic case studies were proposed to describe the main tools and simulation flows offered by IC-EMC. In each case study, simple models were proposed to achieve a reasonable fit between measurements and predictions. The concepts and tools presented in this section will be developed in the following chapters.

2.8 References

[2-1] The analog simulation tool WinSPICE may be downloaded from www.winspice.com.

[2-2] The latest version of the IC-EMC software may be downloaded from www.ic-emc.org.

[2-3] IEC 61967-4: «Integrated circuits, measurement of conducted emissions, 1 Ω/150 Ω method », www.iec.ch

[2-4] A. Boyer, E. Sicard, M. Fer, L. Courau, “Electrical Characterization of a 64 Ball Grid Array Package”, EMC Europe 2008, 8-12 September 2008, Hamburg, Germany

[2-5] IEC 62132-3: “Integrated Circuits, Measurement of Electromagnetic Immunity – 150 KHz to 1 GHz – Part 3: Direct RF Power Injection Method”, www.iec.ch

3 Basic Concepts

Before going deeper in EMC of ICs modeling, some basic concepts should become familiar to analyze rapidly and efficiently some EMC problems. Indeed, reasonable approximations based on a good knowledge of orders of magnitude are most of the time very helpful. Even hard problems can be primarily solved by using judiciously some electrical and physical basic concepts (as interconnection parasitic impedances, impedance matching, spectral contents of signals…). IC-EMC proposes different tools which help the user to better understand these concepts and obtain estimation of EMC related phenomena. The following concepts are required for EMC and are illustrated with IC-EMC:

- Manipulation of EMC major units based on a logarithmic scale expressed in decibels
- Representation of signals in frequency domain and principles of Fast Fourier Transform algorithm
- Fast evaluation of electrical parasitics of passive devices and interconnections
- Plot of impedance of electronic devices versus frequency
- Conditions of matching and effects on signals
- Notions of forward and reflected waves within interconnects
- Characterization of electronic devices through S parameters

3.1 Units

In EMC, the decibel (dB) scale is used as it allows very large or very small values to be represented with a conveniently small number. With a dB scale representation, large and small signals can be plotted or displayed simultaneously without large scale differences. The conversion between linear scale and Decibels is as shown by eq. 3-1. Most values are expressed in dBµV (eq. 3-2). The correspondence between V and dBµV is shown in Fig. 3-1. In IC-EMC, use the command "**Tools → dB/Linear Unit Converter**".

$$V_{dB} = 20.\log(V) \qquad \textit{Equ. 3-1}$$

$$V_{dBuV} = 20.\log(V.10^{6}) \qquad \textit{Equ. 3-2}$$

Where
V=voltage (V)
$V_{dB\mu V}$= voltage in dB micro-volt (dBµV)

The power units are computed in dB-milliwatts (written 'dBm') following the conversion equation 3-3. Notice the coefficient 10 instead of 20 in equ. 3-1 and 3-2.

$$P_{dBm} = 10.\log\left(P.10^{3}\right) = 30 + 10.\log\left(P\right) \qquad \textit{Equ. 3-3}$$

P=power (Watt)
P_{dBm}= power in dB milli-watt (dBm)

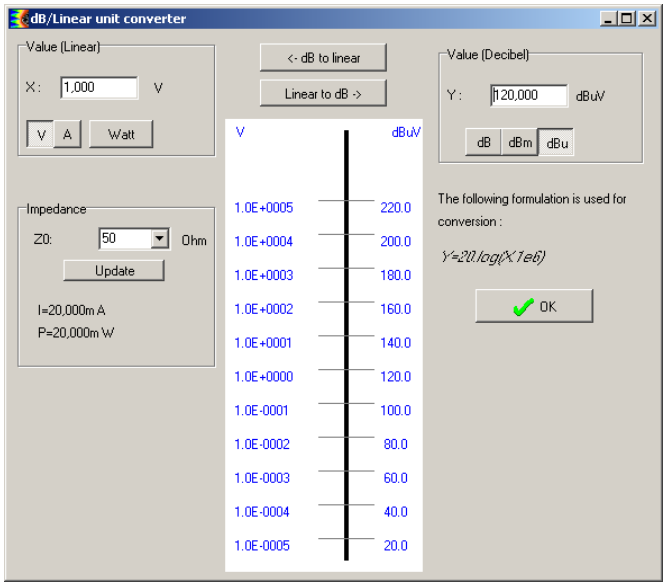


Figure 3-1 : Correspondence between V and dBµV (Tools → dB/Linear Unit Converter)

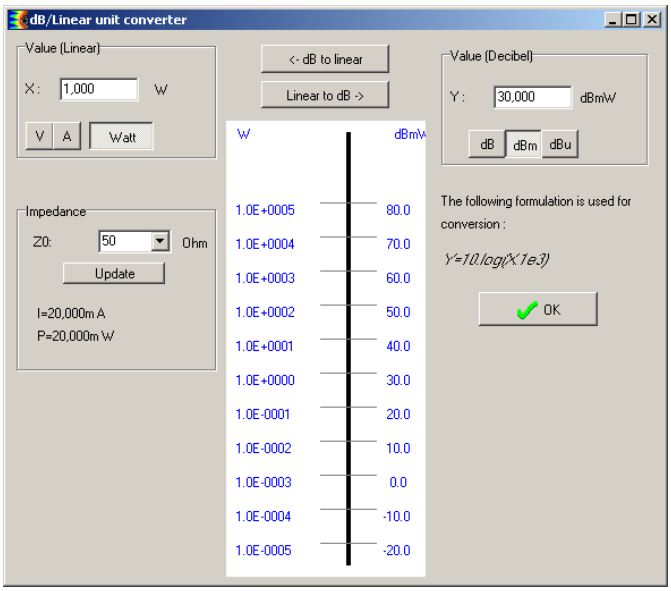


Figure 3-2 : Correspondence between Watt and dBm (Tools → dB/Linear Unit Converter)

3.2 Fourier Transform

EMC performances of integrated circuits are measured using spectrum analyzers rather than oscilloscopes, because of a much higher sensitivity and an ability to separate contribution of small signals in the presence of large ones. Frequency domain is most of the time required to detect distortions of a signal or presence of noise. As we will see in 3.5 (Impedance) and 3.9 sections (S parameters), frequency domain is also very useful for network analysis [3-1].
The conversion between time domain waveform into frequency-domain spectrum is performed using a Fourier Transform. An algorithm called "Fast Fourier Transform" (FFT) makes it possible to carry out the conversion from time domain to frequency domain almost instantaneously. Its drawback is the constraint on the number of samples for x(t), that should be proportional to the power of 2. More information about the implementation of the Fourier Transform in IC-EMC is reported in Appendix F.

3.2.1 Fast Fourier Transform Principles

Let's consider a simple voltage generator loading a 50 Ω resistance (Fig. 3-3). The voltage probe is used to monitor the signal waveform.

1. In IC-EMC, click "File → Open" and select "Basic\FFT\FFT_sinus.SCH" in the list. The schematic diagram of Fig. 3-3 appears.
2. Click "EMC → Generate SPICE". The "FFT_sinus.CIR" text file is generated
3. Invoke WinSpice. Click "File → Open" and load "FFT_sinus.CIR"
4. In IC-EMC, click "EMC→ Voltage vs. Time". Adjust the time and voltage scales by cliking on Auto Fit button or . The following signal appears (Fig. 3-4).

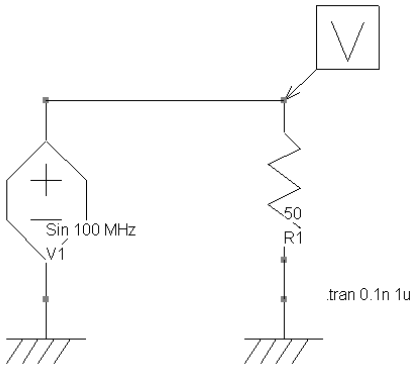


Figure 3-3 : A sinusoidal waveform used to test the Fourier Transform (Basic/FFT/FFT_sinus.SCH)

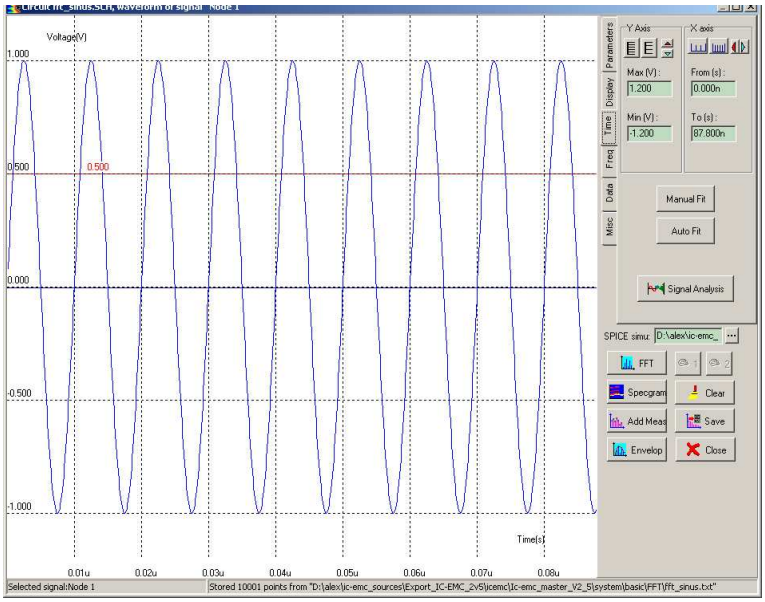


Figure 3-4 : Time-domain aspect of the sinusoidal voltage generator (Basic/FFT/FFT_sinus.txt)

Following a click on "FFT", the Fourier Transform is computed and given in Fig. 3-5. The horizontal axis represents the frequency; the vertical axis represents the *Cn* value such as given in Eq. (3-5). Frequency sampling of this tool is set and starts at 1 MHz and stops at 5 GHz. The main peak of amplitude appearing at a 100 MHz frequency is thus equivalent to a strong *Cn* value. Amplitude of the peak is equal to 120 dBµV. The theoretical value of the fundamental amplitude is equal to 1 V or $20\log(1\,V)+120=120\ dB\mu V$. However, the log/log scale also shows some numeric noise or leakage, i.e the non-zero sub-harmonics on both sides of the main peak.

$$x(t)=a_0+\sum_{n=0}^{\infty}a_n\cos(n\omega_0 t)+\sum_{n=0}^{\infty}b_n\sin(n\omega_0 t)=\sum_{n=0}^{\infty}c_n\exp(jn\omega_0 t) \quad \textit{Equ. 3-4}$$

$$c_n=\frac{1}{T_0}\int_0^{T_0}x(t)\exp(-jn\omega_0 t)dt \quad \textit{Equ. 3-5}$$

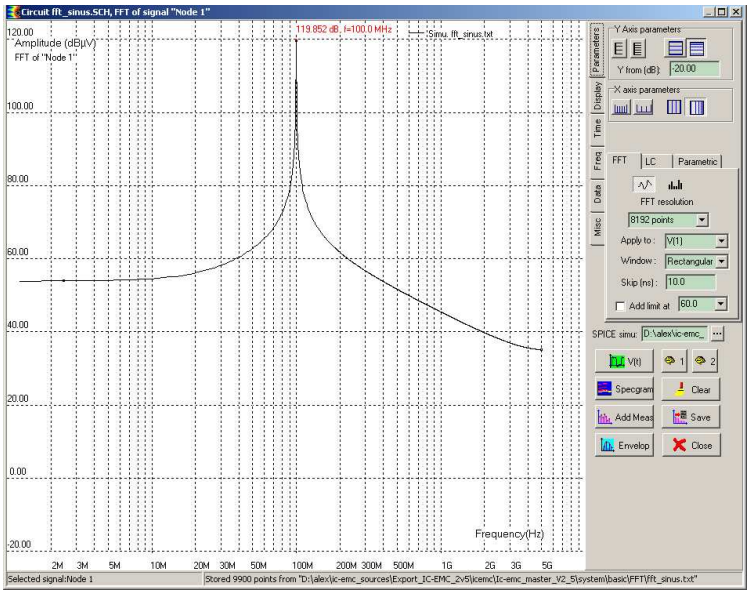


Figure 3-5: Fourier Transform of a sinusoidal waveform (Basic/FFT/FFT_sinus.txt)

These discrepancies with theoretical results come from some undesirable intrinsic properties of FFT. The first limitation of the FFT is the frequency range of the FFT. The minimum frequency of the FFT is given by the frequency resolution or separation between two frequency samples. The frequency resolution is inversely proportional to the signal acquisition time (Equ. 3-6). The maximum frequency is set by the sample frequency of the signal in time domain (Equ. 3-7):

$$F_{FFT\,\min} = \frac{1}{T_{acquisition}} \qquad \textit{Equ. 3-6} \qquad\qquad F_{FFT\,\max} = \frac{F_{sample}}{2} \qquad \textit{Equ. 3-7}$$

The second limitation comes from the limited number of samples or time window upon which the FFT is computed. The FFT algorithm supposes that the input signal is periodic. If an integral of signal period is contained in the time window, then the assumed signal matches with the actual signal (Fig. 3-6).

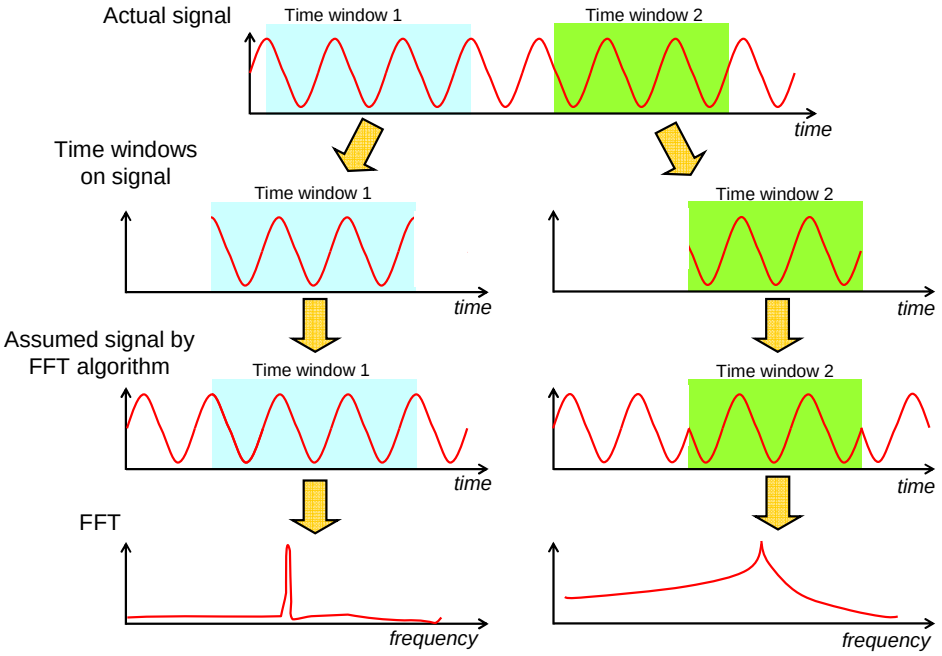


Figure 3-6 : Effect of time window on FFT result

However, if it is not the case, the assumed signal is different from the original signal and presents some sharp discontinuities. These discontinuities have spread frequency content and produce the numeric noise. The numeric noise is particularly important when no special windows are applied. Fig. 3-7 presents the FFT results with a rectangular window. The numeric noise is very high and can mask small signal contribution.
If we set the period of the signal to have an integer number of signal period in the time window, the numeric should collapse. As shown on Fig. 3-5, 8192 samples are used by the FFT. As the sampling period is 0.1 ns, the time window is 819.2 ns long. If the period of the signal is set at 8.192 ns i.e. a frequency of 122.07 MHz, 100 periods of the signal are included in the time window. Figure 3-7 presents the new FFT result. The numeric noise is strongly reduced.

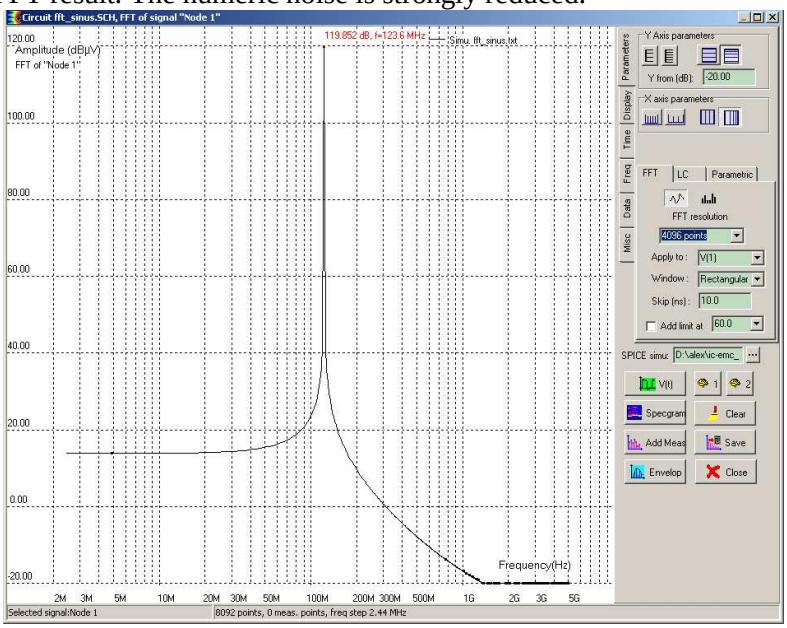


Figure 3-7 : FFT of a sinus signal – an integral number of signal period is contained on the time window of the FFT (Basic/FFT/FFT_sinus.sch)

In order to reduce numeric noise, windowing are applied. It consists in multiplying the signal in the time window by a mathematical function that forces the signal to zero at each bounds of the window, so that the signal can be assumed periodical. Many window types exist. IC-EMC proposes Blackman and Hamming windows (see Appendix F for more details about windowing applied in IC-EMC). Fig. 3-8 and 3-9 present the result of the FFT of a 100 MHz sinusoidal with Hamming and Blackman windows respectively. Compared to FFT without windowing presented in Fig. 3-5, numeric noise is reduced. Only non-zero sub-harmonics appear on both sides of the main peak. Blackman window reduce more considerably the numeric noise than Hamming window, but amplitude of the peak is not significantly affected for both windows.

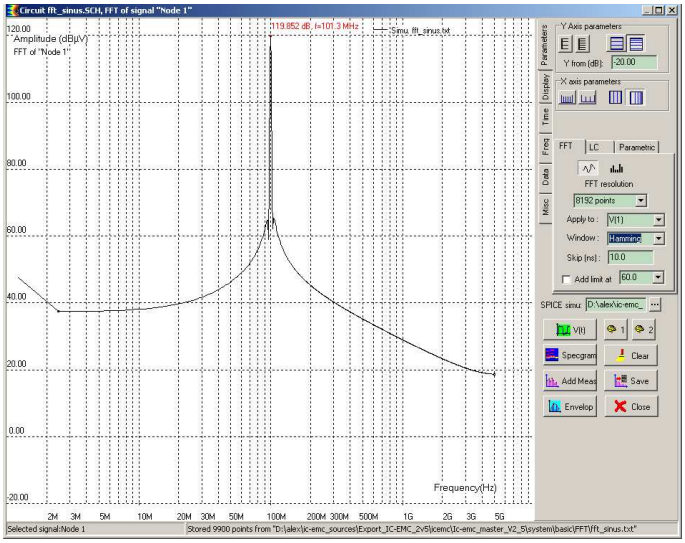


Figure 3-8 : FFT of a sinus signal with a Hamming window – The numeric noise is reduced (Basic/FFT/FFT_sinus.sch)

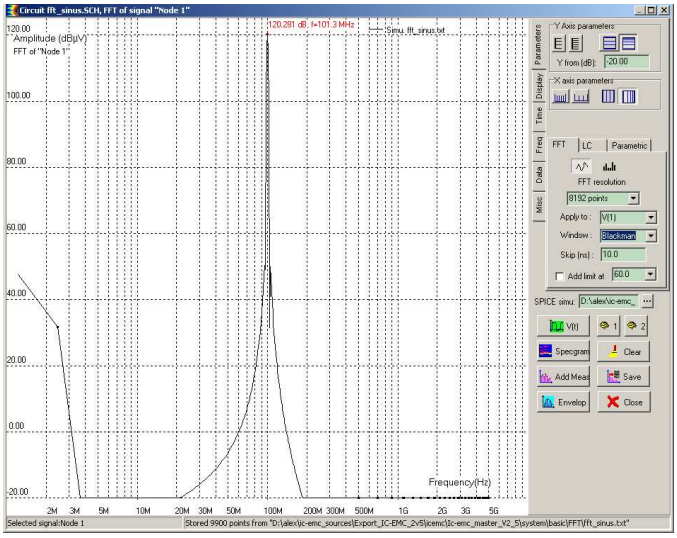


Figure 3-9 : FFT of a sinus signal with a Blackman window – The numeric noise is considerably reduced (Basic/FFT/FFT_sinus.sch)

3.2.2 Spectrum of a rectangular signal

Open the file "Basic/FFT/FFT_rectangular.sch". The Fourier Transform of a pulse signal may be obtained by altering the properties of the voltage source as shown in fig. 3-9. In this case, the Fourier transform of the signal becomes much more complex as it generates not only one peak but an infinite series of harmonics at multiple frequencies of fundamental frequency (10, 20, 30 MHz, etc.) as shown in Fig. 3-10. Even order harmonics are present in the spectrum since the signal is not a symmetrical square signal. The theoretical expression of Fourier coefficient Cn amplitude is given by equation 3-8. A is the signal peak-to-peak amplitude, T is the signal period, τ is the duration at high level, tr is the rise time (we assume that the rise time is equal to the fall time).

$$\left|c_n\right| = \frac{2A\tau}{T}\left|\frac{\sin\left(n\pi\frac{\tau}{T}\right)}{n\pi\frac{\tau}{T}}\right|\left|\frac{\sin\left(n\pi\frac{t_r}{T}\right)}{n\pi\frac{t_r}{T}}\right|, n \geq 0 \qquad \textit{Equ. 3-8}$$

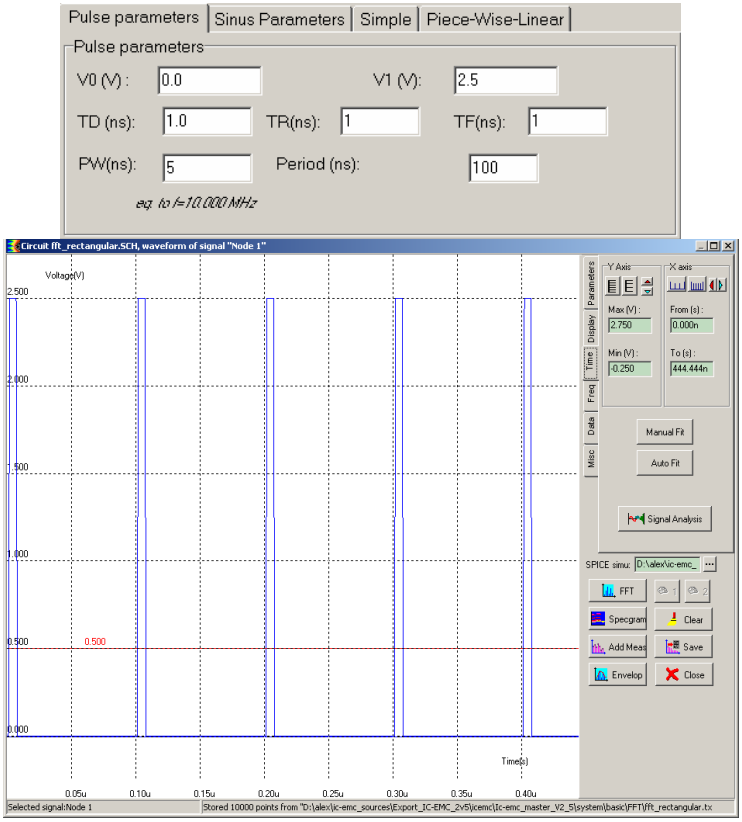


Figure 3-10 : Time domain aspect of a voltage pulse (1 ns rise and fall time, 5ns width, 100 ns period) (Basic/FFT/FFT_rectangular.sch)

Some nulls appear regularly at different frequencies. Theoretically, the spectrum of a rectangular signal characterized by a duty cycle $T_{duty\ cycle}$ and rise (or fall) time T_r presents nulls at multiple frequencies of F_{null1}, which is given by the equation 3-9:

$$F_{null1} = \frac{1}{T_{duty\ cycle}} \qquad \text{Equ. 3-9}$$

Moreover, nulls appear also at multiple frequencies of F_{null2}, which are linked to the rise time and is given by the equation 3-10:

$$F_{null1} = \frac{1}{T_r} \qquad \text{Equ. 3-10}$$

With the defined signal, width of the signal is equal to 6 ns, so that the nulls related to the signal width appears at multiple of 166 MHz. Rise time is equal to 1 ns, so that other nulls appear at multiple of 1 GHz. Amplitude of peaks decrease with harmonic orders and most of the energy is concentrated in the order harmonics. No equation can give the exact bandwidth of a square signal. However, it is directly related to the rise and/or fall time of the signal. Equation 3-11 presents a well-known rule of thumb to estimate the bandwidth F_{BW} of a square, a rectangular and a pulse signal. The upper limit of the bandwidth corresponds to the intersection between the spectrum envelop tangents with -20 dB per decade and -40 dB per decade roll-off slope. For the defined signal, the bandwidth of the signal is about 350 MHz. Most of the energy of the pulse signal is comprised below this frequency [3-2].

$$F_{BW} = \frac{1}{\pi \times T_r} \approx \frac{0.35}{T_r} \qquad \text{Equ. 3-11}$$

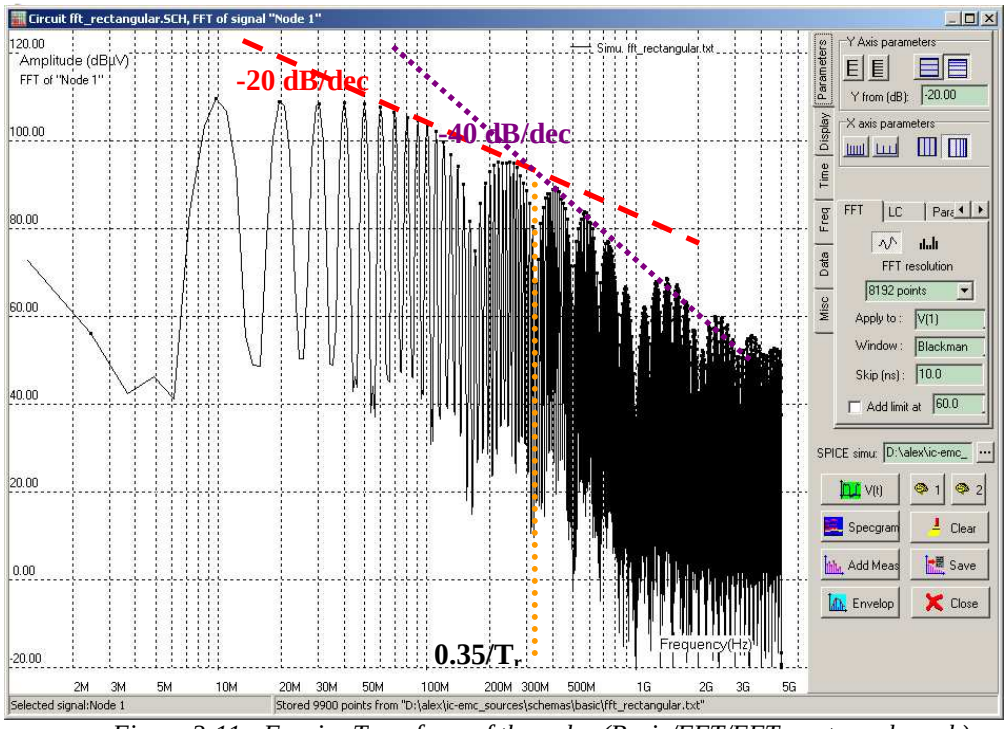


Figure 3-11 : Fourier Transform of the pulse (Basic/FFT/FFT_rectangular.sch)

3.3 Interconnect Model

Integrated circuits are very complex networks made of active and passive devices connected by several layers of interconnections. Each conductor or passive device may be assigned a model based on discrete or local resistances, inductances and capacitances (R,L,C, respectively). This type of model called lumped model is based on the quasi-static approximation, which consists in representing conductor electrical properties by a local passive elements. This approximation is valid in low frequency while the conductor can be considered electrically small compared to the wavelength of the considered frequency. A typical criterion to evaluate the frequency limit of the quasi-static approximation is that the length of the conductor is smaller than the tenth of the wavelength of the considered signal [3-3].

$$length\ conductor < \frac{\lambda}{10} = \frac{c}{10\sqrt{\varepsilon_r}\, f} \qquad \text{Equ. 3-12}$$

EMC problems are often related to unexpected current return paths due to uncontrolled interconnection impedances. Solutions of most of EMC problems are based on a reasonable estimation of parasitic elements of interconnections. Even if conductor parasitic elements remain negligible at low frequency, this assumption is not valid at higher frequencies and underestimations can be dramatic to prevent EMC issues.
In EMC of ICs, the conductors of utmost importance are:

- The on-chip decoupling capacitance
- The on-chip serial resistance of the supply networks
- The package inductance

We detail in this section how to evaluate these parameters.

3.3.1 Interconnect Parameters

The “Interconnect parameters” tool included in the **Tool** menu computes the R,L,C parameters of an

interconnect based on its physical dimensions. Analytical formulations detailed in appendix G are used for these evaluations.

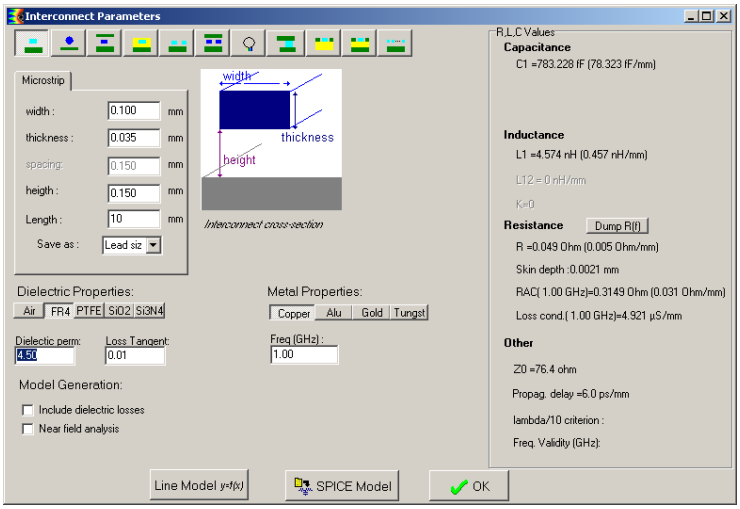


Figure 3-12 : Interconnect R,L,C model based on physical dimensions (Tools → Interconnect Parameters)

IC-EMC proposes the following electrical parameters, depending on the interconnect type: lineic and total resistances (DC and AC, AC resistance takes into account skin effect), lineic and total inductance and capacitance, lineic direlectric losses, mutual inductance and capacitance, characteristic impedance, propagation delay.

3.3.1.1 Interconnect electrical model

propose to build the electrical model of two coupled interconnects. The dimensions of these interconnect are typical of leads of package such as Quad Flat Package (QFP):

- width of interconnects = 0.25 mm
- thickness of interconnects = 0.1 mm
- spacing between interconnects = 0.25 mm
- height to ground plane = 0.7 mm
- length of interconnects = 10 mm
- dielectric constant = 4.5
- metal = copper
- limit of validity of the model = 2 GHz

Click on “Tools → Interconnect parameters”. The interface dedicated to the definition of interconnects geometry and generation of electrical model opens. Click on the button “Two conductors above ground” or  and enter the previous geometrical parameters, as shown in figure 3-13.

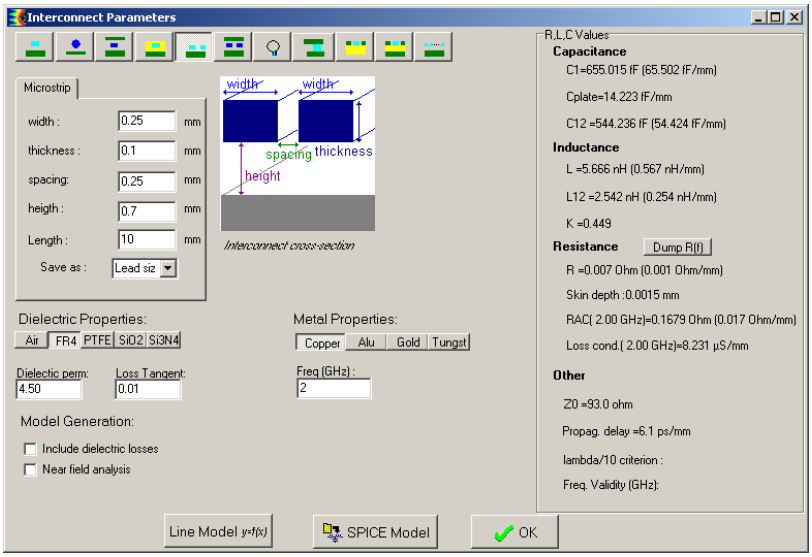


Figure 3-13 : Electrical parameters per length of 2 coupled lines and automatic generation of a SPICE model

Then, click on the button “Apply y=f(x)” to compute interconnects electrical parameters per length. Formulations used to compute resistance, inductance and capacitance per length are detailed in appendix G. Results appear on the right column of the interface. A SPICE model of these 2 coupled lines can be automatically generated in the schematic editor by clicking on the button “SPICE Model”. Finally click on the button “OK” to return on the schematic editor. Figure 3-14 illustrates the generated model. This is a lumped model, each RLC cell models a λmin/10 long element of the interconnect, where λmin is the minimum wavelength. As the maximum frequency of validity of this model is set to 2 GHz, the maximum physical length of each RLC cell is equal to 7 mm, so that two RLC cells are required to model the interconnects.

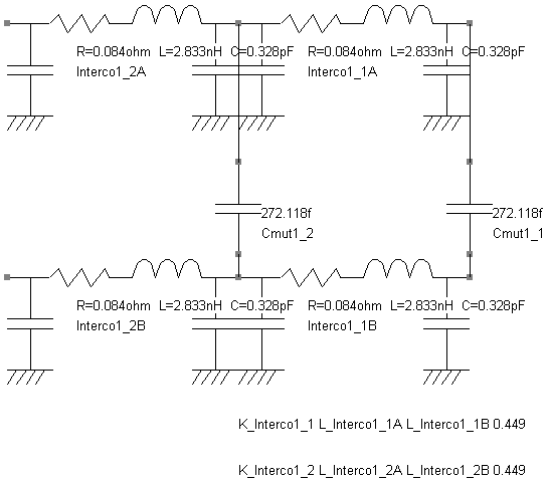


Figure 3-14 : Lumped model of two coupled lines automatically generated by the tool Interconnect Parameters

The model of the coupled interconnects is included in the file “Basic/interconnects/CoupledInterconnects.sch”. Figure 3-15 describes the model. The two interconnects are loaded by 10 pF capacitors which are typical of input capacitance of CMOS circuits. On of these lines is connected to a 50 MHz square signal generator which represents an ideal switching CMOS circuit output. A serial 10 Ω resistor is added to improve the termination of the line [3-4]. The other line is loaded in the same way except that the output buffer does not switch and the extremity of the line is connected to the ground.

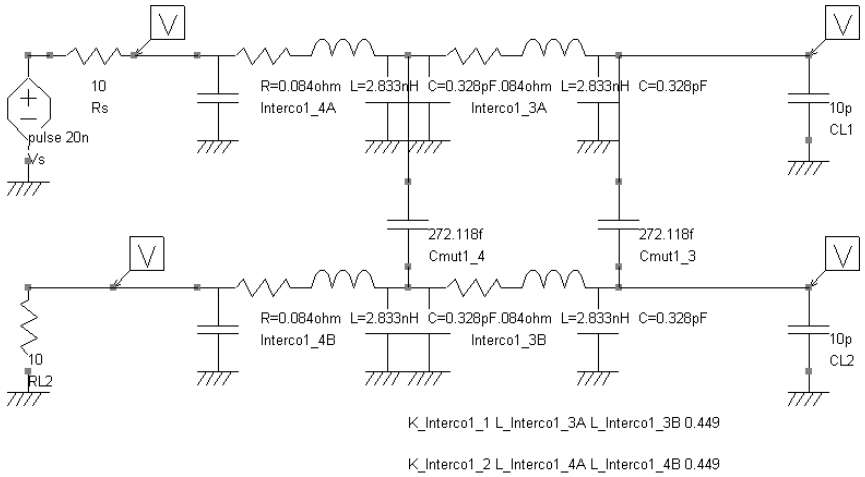


Figure 3-15 : Model of two coupled and loaded interconnects ("Basic/interconnects/CoupledInterconnects.sch")

The rise and fall time of the square signal is first set to 2 ns. A transient simulation is performed to extract the transient waveform at each terminals of both coupled interconnects. Figure 3-16 presents the WinSPICE simulation result. A small ringing appears after each transitions on the input and output signal of the line connected to the generator. This ringing is due to the unmatched condition of the line. Matching issues are discussed in part 3.6. The pseudo period of the ringing is linked to total capacitance and inductance of the line and load. The overshot is more important at the receiver side. On the coupled line, a part of the signal which propagated along the other line is coupled and some ringing appears also. This effect is called crosstalk.

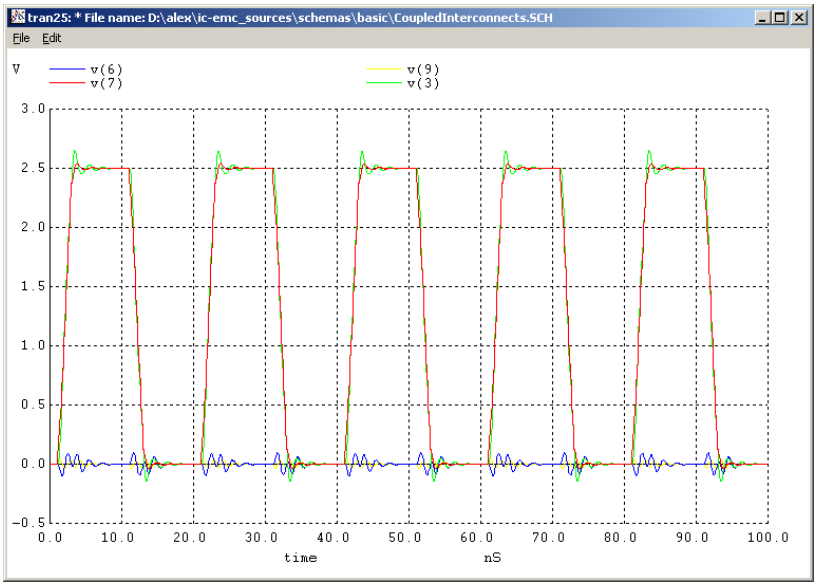


Figure 3-16 : Transient waveform at each terminals of the coupled interconnects, Tr=Tf = 2 ns ("Basic/interconnects/CoupledInterconnects.sch")

Set the rise and fall time to 100 ps and launch the WinSPICE simulation. Figure 3-17 presents the simulation result.

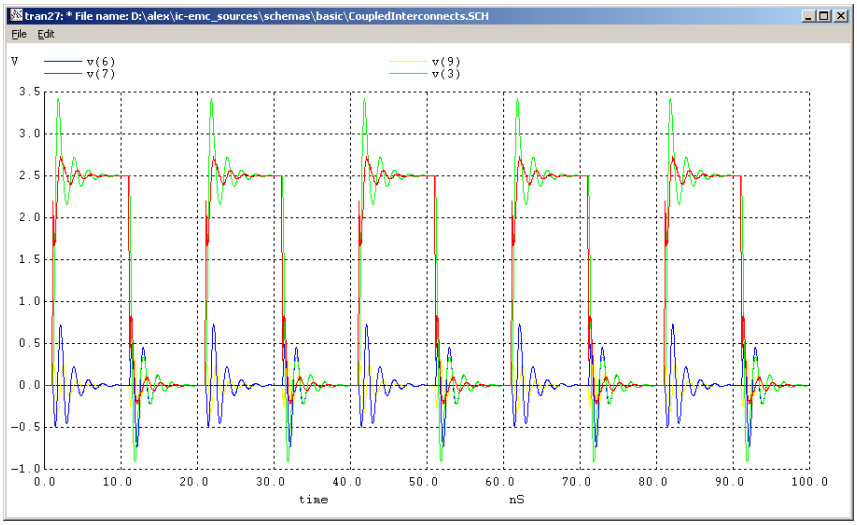


Figure 3-17 : Transient waveform at each terminals of the coupled interconnects, Tr=Tf = 100 ps ("Basic/interconnects/CoupledInterconnects.sch")

The ringing gets worse when the rise and fall times are reduced. The overshoot observed across the capacitor is almost 1 V. The amplitude of the crosstalk is also larger and reach 700 mV. As the rise or fall time decreases, the effect of propagation along the interconnects become more significant. From an electrical point of view, if the rise time decreases, the capacitance load must be charged quickly, so that the di/dt becomes larger. As interconnects are mainly inductive, it increases the voltage bounce along the interconnects.

3.4 L,C Resonance

The combination of inductance (mostly the package inductance) and the capacitance (mostly the IC on-chip capacitance) creates a resonance at a frequency given by Equ. 3-13.

$$f_r = \frac{1}{2\pi\sqrt{L.C}} \qquad \textit{Equ. 3-13}$$

fr= resonant frequency (Hz)
L=inductance (Henry)
C=capacitance (Farad)

The relationship between usual capacitance, inductance values as found in integrated circuits and the resonant frequency is plotted in the abacus proposed in Fig. 3-18. For these graphs, we just applied equation 3-13. Knowing the package inductance and on-chip capacitance, we may deduce the corresponding resonant frequency.
The command "**Tools → Resonant Frequency**" tool proposes a menu to compute the impedance of L, C at a given frequency. The LC resonance is also computed, with its associated characteristic impedance (Figure 3-19).

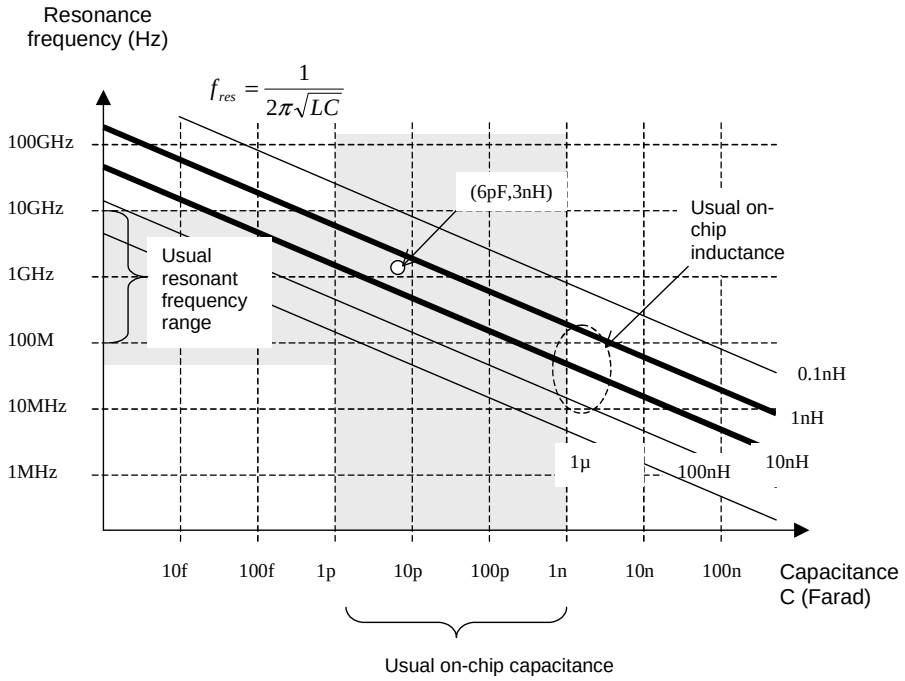


Figure 3-18 : Relationship between usual capacitance, inductance and resonant frequency.

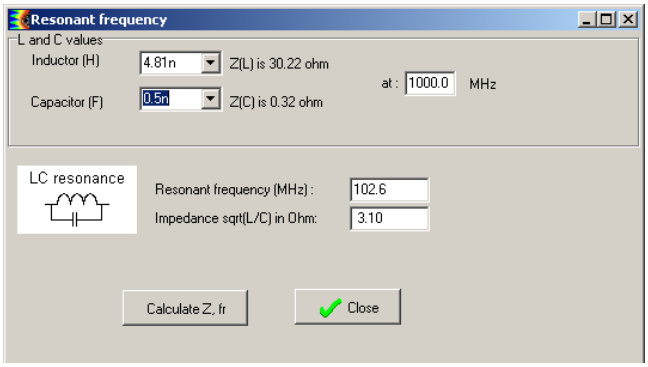


Figure 3-19: Resonant frequency of given L and C, with associated impedance

The quality factor Q is a metric to quantify the resonance effect. It implies not only L and C elements but also a resistance. One formulation for the quality factor is proposed in Equ. 3-14. We consider one inductor L, a resistor R, and one capacitor C.

$$Q = \frac{\sqrt{\frac{L}{C}}}{R} \qquad \textit{Equ. 3-14}$$

3.5 Impedance

3.5.1 Introduction

The basic elements presented in the previous section have strong frequency dependence. The variation of impedance at IC level is quite complex, specifically at high frequencies. An example of IC supply impedance measurement performed on an Atmel C51 microcontroller is proposed in Fig. 3-20.

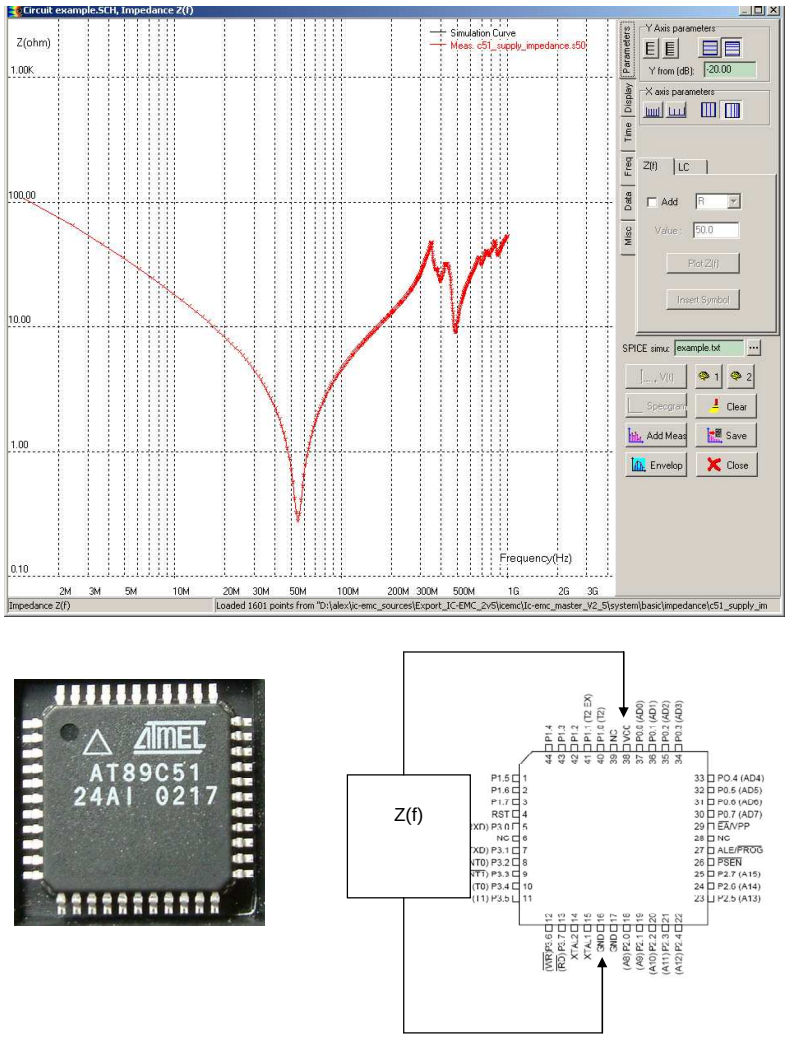
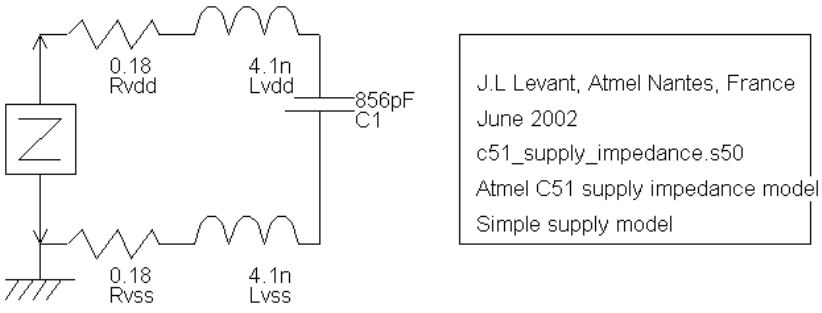


Figure 3-20: Impedance measured between VDD and VSS supply pins (basic/impedance/ c51_supply_impedance.s50)

3.5.2 Impedance simulation

An example of IC power supply models produced with IC-EMC is shown in figure 3-21. The model is made of discrete passive elements. The supply impedance of the integrated circuit is represented by the on-chip decoupling *C1*, the access package inductance *LVdd*, *LVss*, as well as parasitic serial resistance *Rvdd* and *Rvss*. The software uses a specific probe called "Z probe" that can be found in the probe menu, close to the voltage probe. The Z probe is inserted between the two electrical nodes where the impedance needs to be measured.



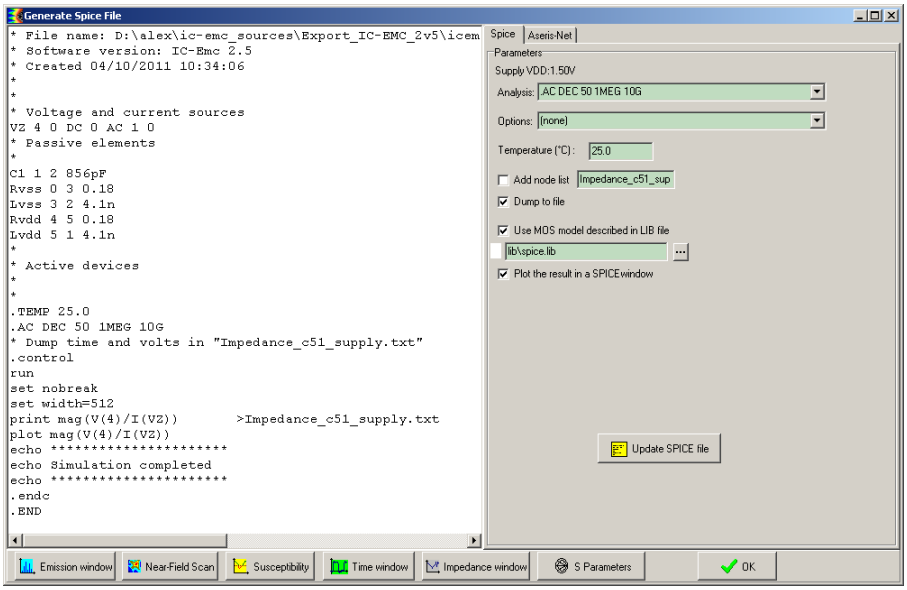


Figure 3-21: The impedance simulation in IC-EMC uses a specific Z probe (basic/impedance/ Impedance_c51_supply.sch)

1. Generate the Spice file (as appearing in Fig. 3-21)
2. Start WinSpice, click File → Open and select the file"*impedance_c51_supply.CIR"*. The AC simulation is started, and the output file is *impedance_c51_supply.TXT*. It contains the module of the impedance.
3. Click "Impedance Window" or "EMC→ Impedance vs. Frequency"
4. Select the button "Add measurements", select the data format "s50". Click "c51_supply_impedance.s50". The comparison is shown in figure 3-22.

The simulator uses an AC Source combined with a probing of the current. The result is plotted on a specific window by a click in "Impedance Window" from the Spice interface (Figure 3-22). The ratio between the voltage and current has been automatically computed from 10 MHz to 10 GHz, as declared in the Spice netlist. The correlation is quite good up to 200 MHz. Resonances measured at 300 MHz and 500 MHz would need more discrete R,L,C elements to move at higher frequency the limit of validity of the quasi-static approximation.

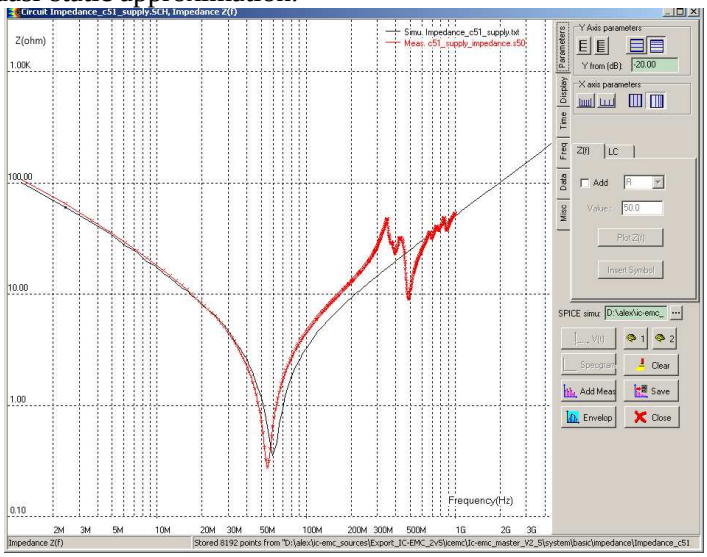


Figure 3-22: Impedance simulation result compared with impedance measurement (basic/impedance/c51_supply_impedance.s50)

3.5.3 Impedance Identification

Given an impedance profile, the identification of R,L,C elements is relatively easy. For illustration purpose, let us consider the data file “passive\capa100pf\capa_100pF_S22.s50”, corresponding to a [s] measurement of a 100 pF discrete surface-mounted capacitor. The measurement appears in red in fig. 3-23. Select the “Add” item, select “C” in the list and click in the measurement curve on the left part as indicated (Item 4). Then click “Plot Z(f)”. The green curve appears, which corresponds to Z(f) of a 107-pF capacitor. Click “Insert Symbol” to instantiate directly the corresponding symbol in the schematic diagram.

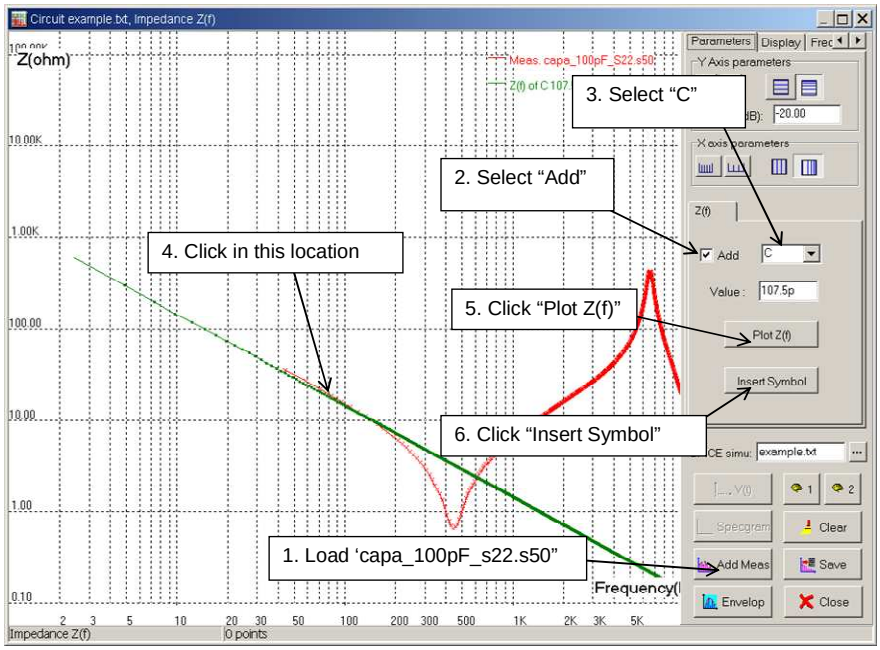


Figure 3-23 : Impedance identification (based on “passive\capa100pf\capa_100pF_S22.s50”)

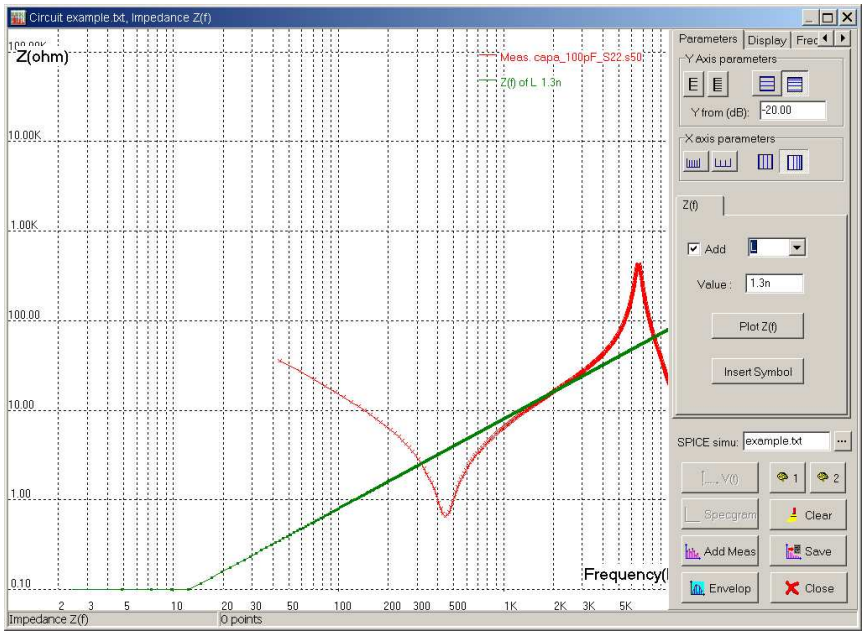


Figure 3-24 : Identification of the high-frequency parasitic inductance (“passive\capa100pf\capa_100pF_S22.s50”)

The other elements are a 1.2-nH inductance and a 0.5pF capacitance. A serial and a parallel resistances can be added to tune the amplitude of both resonances. The final model is shown Fig. 3-25. It includes 5 parasitic elements in addition to the desired 100-pF capacitor. Correlation with measurement is

presented on figure 3-26.

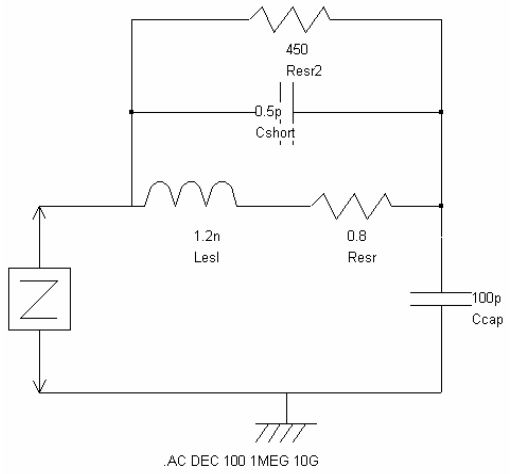


Figure 3-25 : Model of the 100 pF capacitance tuned from measurement ("capa_100pF_S22_tune.SCH")

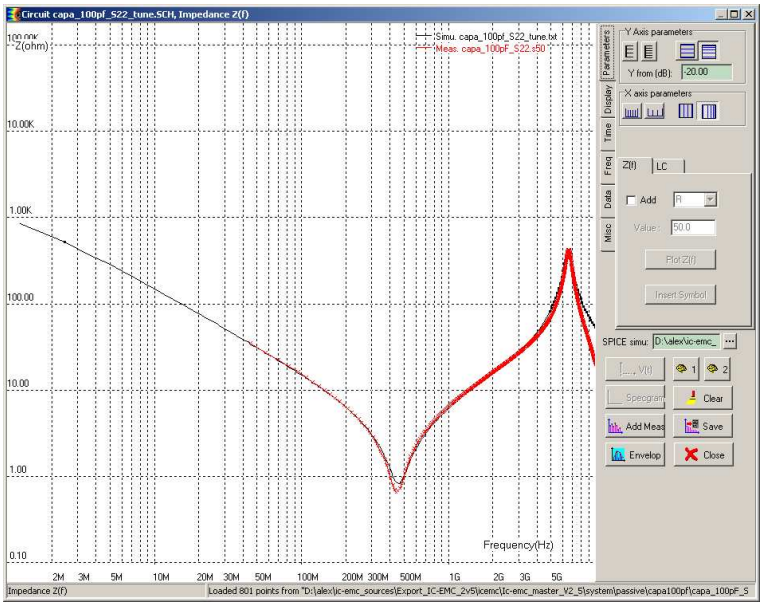


Figure 3-26 : Comparison between measurement and simulation of the 100 pF capacitance ("capa_100pF_S22_tune.SCH")

3.6 Impedance Matching

Most EMC equipments use 50 Ω cables and 50 Ω loads for impedance matching. We illustrate in this section the problem of using cables and high impedance oscilloscope to measure high frequency signals provided by a CMOS buffer. We start by simplifying this buffer by an equivalent pulse generator to induce the switching of the CMOS buffer. The buffer loads a 1-m transmission line, corresponding to an ideal cable with characteristics impedance of 50 Ω. The transmission line is connected to a 1-MΩ load, which represents the input impedance of an oscilloscope. In SPICE, the "M" means "milli", the "MEG" means MEGA. We add two probes to compare the near-end and far-end signal waveform. The complete schematic diagram is proposed in Fig. 3-27.

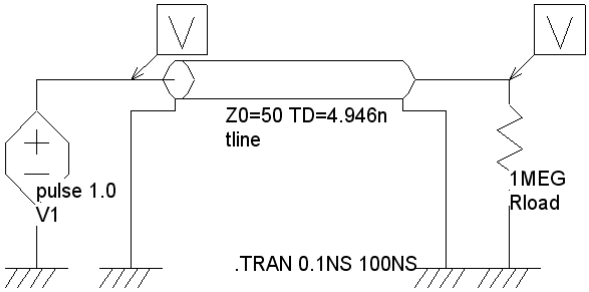


Figure 3-27 : A simplified buffer loads a 1-m cable and a 1MEG termination (basic\impedance\impedance_mismatch.SCH)

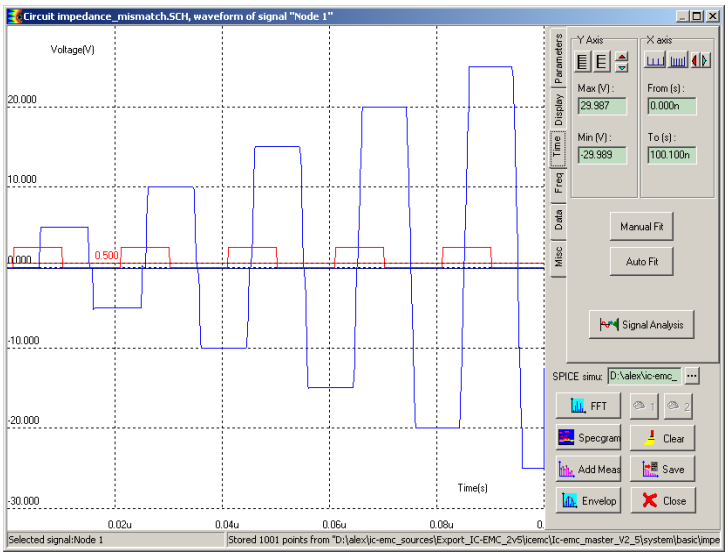


Figure 3-28 : SPICE simulation with unmatched load (basic\impedance\impedance_mismatch.SCH)

The simulation appearing in Fig. 3-28 shows an important distortion of the original signal. This is due to the 1MΩ termination which induces a signal reflection through the cable. More explanations about reflection are provided in the next part. When changing this 1 MΩ load into a 50 Ω load, the waveform becomes much closer to what was expected (Fig. 3-29). Signal is transmitted to the load without any distortions.

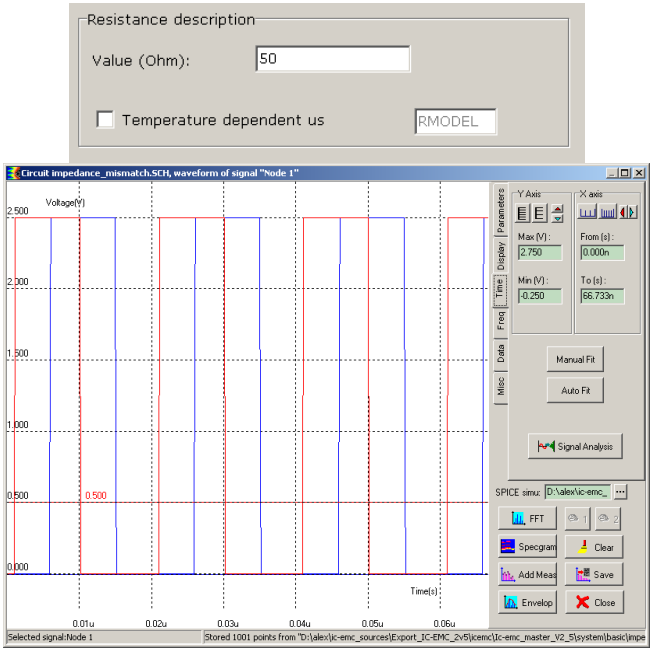


Figure 3-29 : 1-m cable with matched termination (basic \impedance \impedance_mismatch.SCH)

The same example can be done with a more realistic model of a CMOS output buffer. The buffer is made of one NMOS and PMOS devices mounted as an inverter. Model of transistors is included in a library file called “spice.lib”. The pulse voltage source supplied the input of the CMOS buffer. Two probes are placed at each ends of the cable to compare near-end and far-end signals. The schematic is presented in Fig. 3-30.

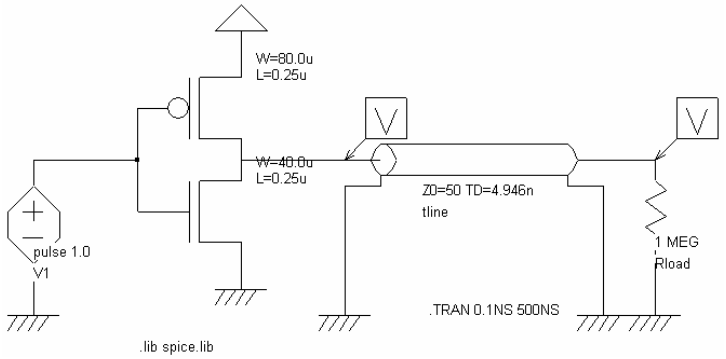


Figure 3-30 : A CMOS buffer loads a 1-m cable and a 1MEG termination (basic\impedance\impedance_mismatch_buffer.SCH)

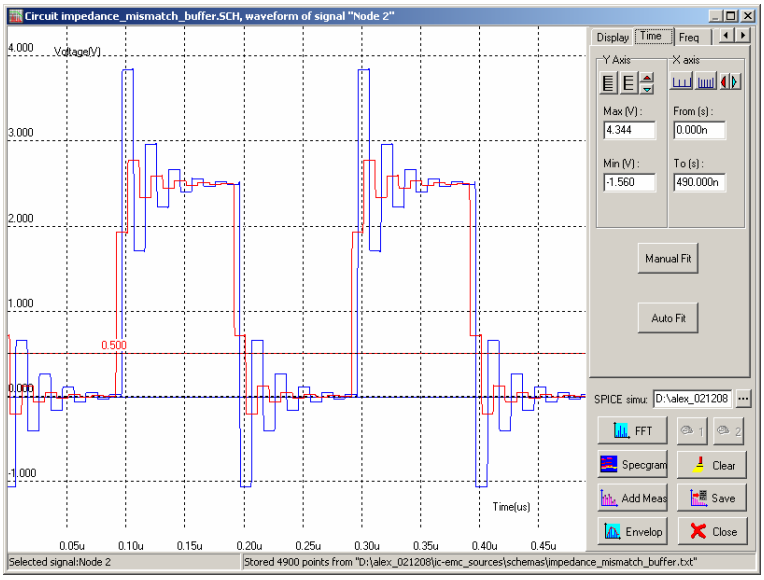


Figure 3-31 : SPICE simulation with unmatched load (basic\impedance\impedance_mismatch_buffer.SCH)

The simulation results presented in Fig. 3-31 shows ringing oscillations which appear after each transition, due to reflected signal by the mismatch at the end of the cable. These parasitic oscillations can be misunderstood by digital input buffers as a logical state change. Half period of these oscillations are equal to twice of the propagation delay in the cable. Unmatching can have dramatic consequences on digital signal integrity, especially for high speed digital signal transmissions. As expected, changing the 1 MΩ to a 50 Ω load leads to a matching condition and prevents from signal distortions, as shown in figure 3-32.

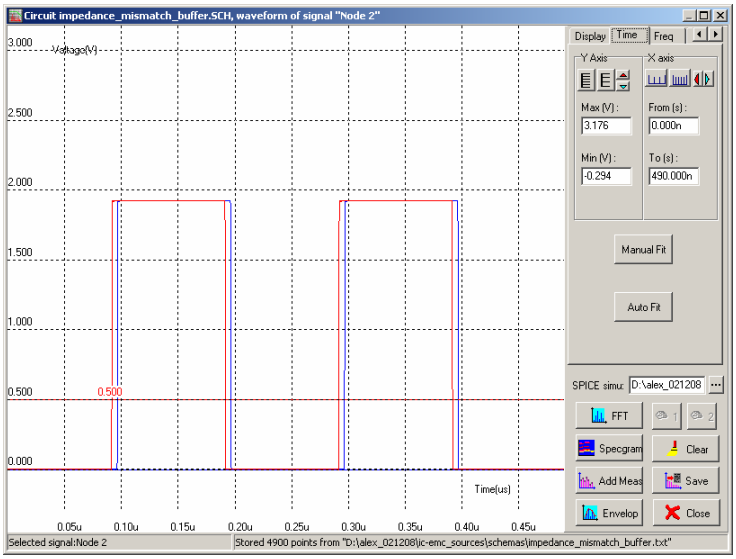


Figure 3-32 : Signals at near-end and far-end of 1 m cable supplied by a CMOS buffer and ended by an matched termination (basic\impedance\impedance_mismatch_buffer.SCH)

3.7 Power matching

Impedance matching is not only fundamental for signal integrity but also for power transfer. The following schematic is proposed to illustrate the power matching condition. Here, we only consider the case of resistive load. It is composed of a resistive load R_{load} connected to a generator modeled by a voltage generator Vs and an internal resistor Rs. A voltage probe is placed at one node of the load. The probe will be configured to sense the power transferred to the resistive load. Double click on the probe and select the option "dBm (on a fixed resistor)". A field appears to define the resistor value on which the power is computed. An AC simulation is set to compute the power amplitude over a frequency band.

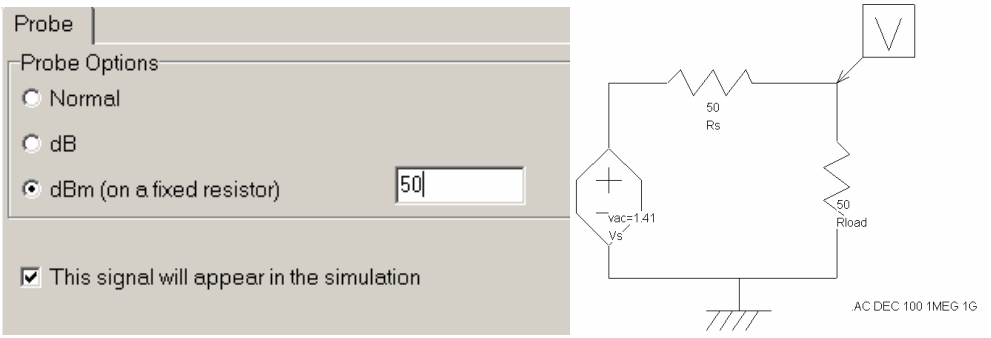


Figure 3-33 : Illustration of the power matching condition (basic\power\power_match.SCH)

Theoretically, the power delivered by the voltage source to the load is given by the following equation.

$$P_{Load} = R_{Load} \times I_{Load}^2 = \frac{R_{Load} \times V_S^2}{\left(R_{Load} + R_S\right)^2} \quad \textit{Equ. 3-15}$$

For a given source resistor, there exists a load resistor value for which the power transfer to the load is optimized. This condition corresponds to the power matching condition and is met when the load resistor is equal to the source resistor. In this condition, the power delivered by the source to the load is equal to the maximum available power P_{av} (Equ. 3-20).

$$P_{av} = \frac{R_S \times V_S^2}{\left(R_S + R_{Load}\right)^2} = \frac{V_S^2}{4R_S} \quad \textit{Equ. 3-16}$$

In the circuit described in Fig. 3-33, the source voltage amplitude is equal to 1.41 V and the source

resistor is equal to 50 Ω. According to Equ. 3-16, the maximum available power of the source is equal to 10 mW i.e 10 dBm. Simulation of the power delivered to a 50 Ω load confirms that it is equal to the maximum available power (Fig. 3-34).

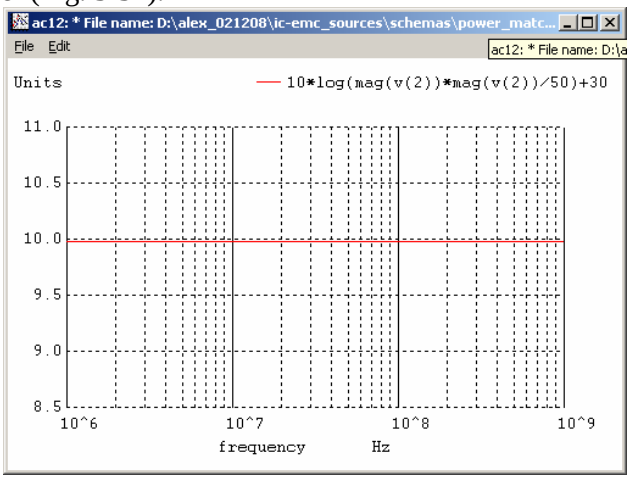


Figure 3-34 : Power delivered to the load for power matching condition (basic\power\power_match.CIR)

In order to confirm that the maximum power is transferred to the load when power matching condition is met, change the value of resistor, e.g. 10 and 200 Ω. Remind that you have to change the resistance property of the voltage probe. Fig. 3-35 presents the simulation results. Power delivered to the load is respectively equal to 7.5 and 8 dBm.

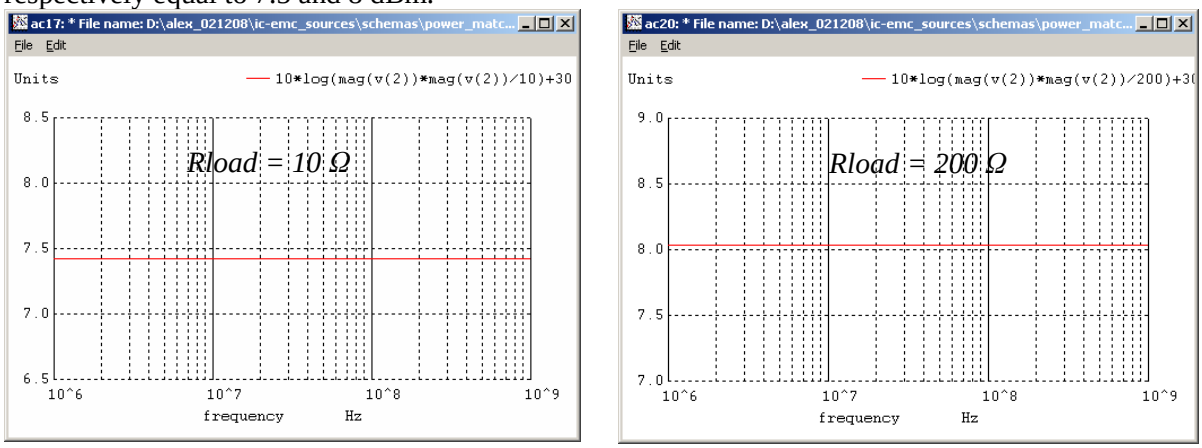


Figure 3-35 : Power delivered to the load when power matching condition is not met (basic\power\power_match.CIR)

3.8 Forward and Reflected Voltage

Analysis of transmission lines shows that voltages and currents in any points of the lines corresponds to the superposition of two waves traveling in opposite directions. The incoming wave is called forward wave while the outcoming wave is called reflected wave. These two waves do not interact except at the boundaries of the lines, where some conditions are set by terminal impedances. Fig. 3-36 illustrates these concepts. Consider the case of a load connected to a RF source through a cable with characteristic impedance *Zc*. The load and the source are characterized by complex impedances *Zload* and *Zsource*. Suppose that the origin of the cable (x=0) is set on the load position.

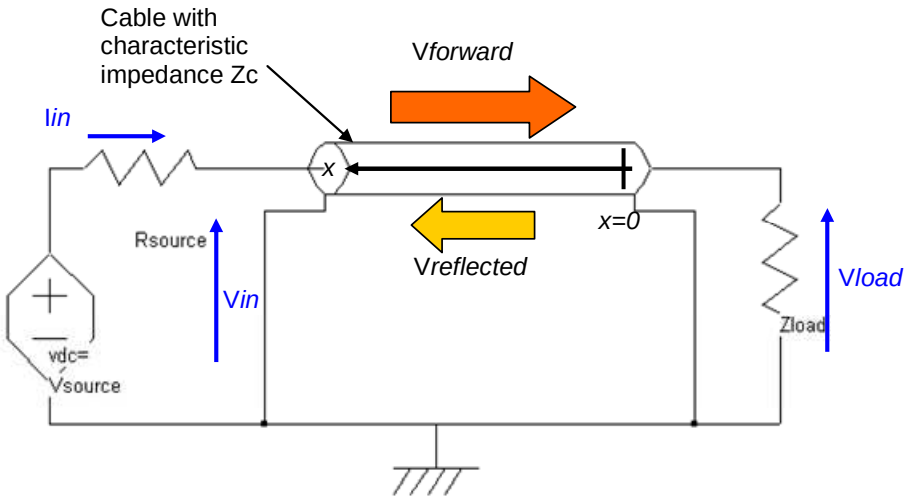


Figure 3-36 : Coexistence of a forward and a reflected wave along a transmission line

The voltage at each point x of the cable results from the superposition of forward *Vforw* and reflected *Vrefl* voltages (equation 3-17). The variable γ is the propagation constant in the cable. Thus, at x=0, the voltage on the load can be deduced from equation 3-18.

$$\overline{V}(x) = \overline{V}_{forw} \exp(\gamma x) + \overline{V}_{refl} \exp(-\gamma x) \quad \textit{Equ. 3-17}$$

$$\overline{V}(0) = \overline{V}_{load} = \overline{V}_{forw} + \overline{V}_{refl} \quad \textit{Equ. 3-18}$$

By combining expressions of voltage and current at the line input, expressions for forward and reflected voltage can be deduced:

$$V_{forward} = \frac{V_{in} + Z_c \times I_{in}}{2} \quad \textit{Equ. 3-19}$$

$$V_{reflected} = \frac{V_{in} - Z_c \times I_{in}}{2} \quad \textit{Equ. 3-20}$$

At interfaces between lines and termination impedances, voltages and currents must be continuous, so that some boundary conditions must be fulfilled. These conditions can be described in terms of reflection coefficient Γ. As shown by equation 3-21, the reflection coefficient Γ is the ratio between the reflected and forward voltages. However, as Γ depends on termination impedances and the characteristic impedance of the line (equation 3-22), forward and reflected voltages are linked together with the impedance boundaries of the line. As explained in the previous parts, the existence of the reflected voltage results in signal integrity degradations. Canceling the reflection coefficient by matching cable terminations is the only condition to prevent from signal degradations. This condition should be met at both terminations of the line: source and load impedance matched on the line impedance.

$$\Gamma = \frac{|V_{refl}|}{|V_{forw}|} \quad \textit{Equ. 3-21}$$

$$\Gamma = \frac{Z_{load} - Z_C}{Z_{load} + Z_C} \qquad \textit{Equ. 3-22}$$

In order to illustrate the previous concepts, we can use the TDR symbol, available in ieee\TDR.sym. The symbol can be inserted in the schematic by clicking on Insert → User Symbol (.SYM).
A TDR (Time Domain Reflectometry) is an equipment used to check the impedance uniformity along a conductor, its principle is very similar to a radar (Fig. 3-37). A TDR transmits a pulse through a conductor and senses the voltage waveform at the conductor input in the time domain. If the conductor presents no discontinuities and is terminated by a matched load, no reflected voltage returns toward the TDR, so that the TDR input/output voltage waveform is not altered by the reflected voltage and equal to the forward voltage.
However, any impedance discontinuities along the conductor will induce a reflected voltage. The reflected voltage will be sent back to the input/output of the TDR after two times the line delay and will affect the waveform measured by the TDR. A TDR is characterized by a short rise time pulse. The shorter the rise time, the better is the TDR resolution, i.e. the ability to detect small discontinuities along the conductor.

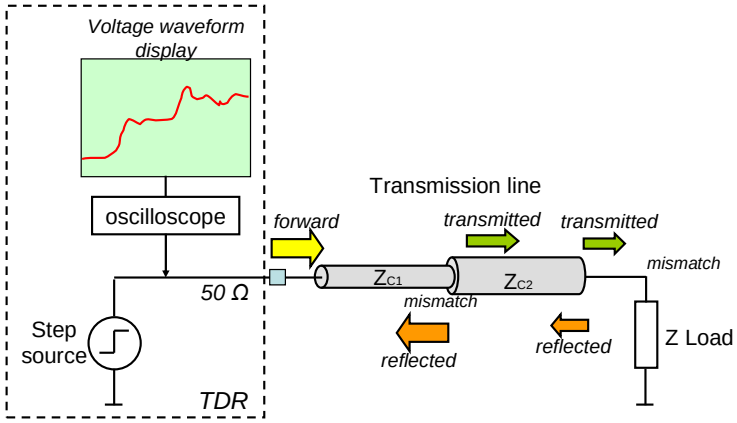


Figure 3-37 : Illustration of the principle of a TDR

3.8.1 TDR on an unmatched load

Open the file called "basic\TDR\reflection_load.sch" (Fig. 3-38). A resistive load is connected to a TDR by a 50 Ω line. Double click on the TDR symbol to reach its properties (Fig. 3-39). Properties of the TDR pulse (amplitude, rise time and pulse width) and the output impedance can be modified. The amplitude of the TDR pulse corresponds to a specified one only if the TDR impedance is matched to the line impedance.

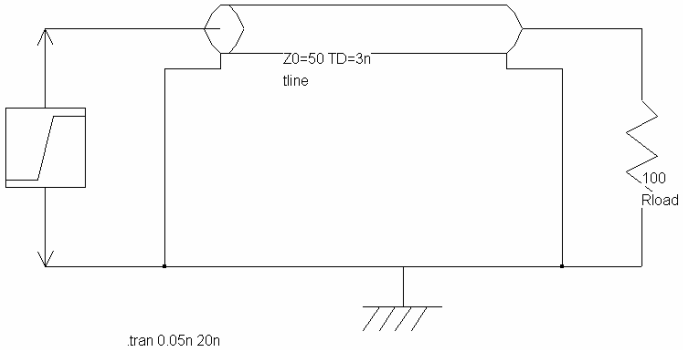


Figure 3-38 : Illustration of the reflected voltage (basic\TDR\reflection_load.sch)

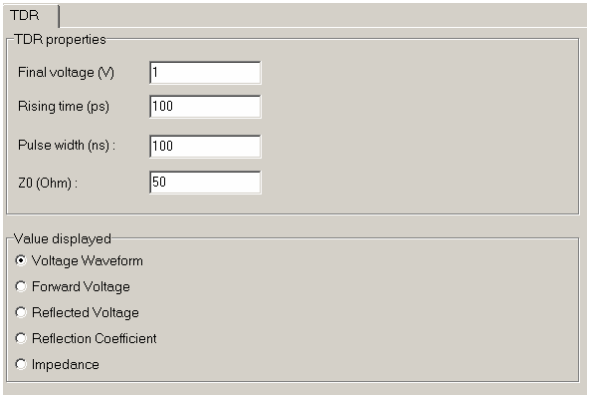


Figure 3-39 : TDR symbol properties

Several parameters can be computed when the TDR symbol is placed in the schematic diagram: the voltage waveform at the input/output of the TDR, the forward voltage, the reflected voltage, the reflection coefficient and the impedance versus time. A transient analysis must be set to allow a TDR simulation. Select "Voltage waveform", set the load impedance to 25 Ω and then to 100 Ω. Figure 3-40 presents the simulation results for these two load resistor values.

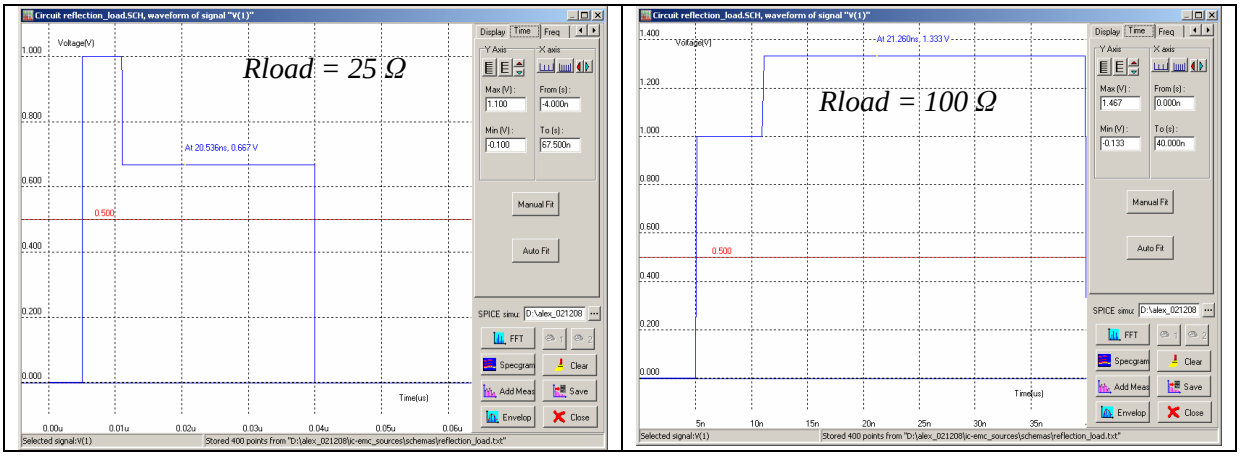


Figure 3-40 : Simulation of the waveform at the input/output of the TDR for a 25 Ω (on the left) and a 100 Ω (on the left) load (basic\TDR\reflection_load.sch)

At 10 ns, the TDR generates a pulse and a 1 V voltage is measured at the output of the TDR. The voltage remains constant for 6 ns (2 times the delay of the line). During this period the forward wave travels to the load. When it reaches the load, a part of the incident energy is reflected, causing a change of the input/output TDR waveform when the reflected wave reaches the source. As shown in Fig. 3-41, if the load resistance is less than the characteristic impedance, the reflected wave is out of phase of the forward wave and reduces the amplitude of the original pulse. Conversely, if the load impedance is higher to the characteristic impedance, the reflected wave is in phase with the forward wave and reinforces the amplitude of the original pulse. As the TDR source impedance is matched with the line impedance, no reflection occurs at the line input so that the waveform remains steady.

In the case of a 25 Ω load, the reflection coefficient is equal to $-\frac{1}{3}$. When the reflected wave reaches the TDR output, the waveform voltage amplitude is equal to:

$$V_{in}(t=6ns)=V_{forw}(t=6ns)+V_{refl}(t=6ns)=1-\frac{1}{3}=0.66\,V$$

In the case of a 100 Ω load, the reflection coefficient is equal to $+\frac{1}{3}$. When the reflected wave reaches the TDR output, the waveform voltage amplitude is equal to:

$$V_{in}(t=6ns)=V_{forw}(t=6ns)+V_{refl}(t=6ns)=1+\frac{1}{3}=1.33V$$

The TDR also offers the option to plot the reflection coefficient versus time seen from the input/output of the TDR (Fig. 3-43). During 6 ns, the reflection coefficient is equal to zero as no reflected wave reach the TDR input. After 6 ns, a continuous reflected wave travels from the load to the TDR so that the reflection coefficient is equal to 0.33.

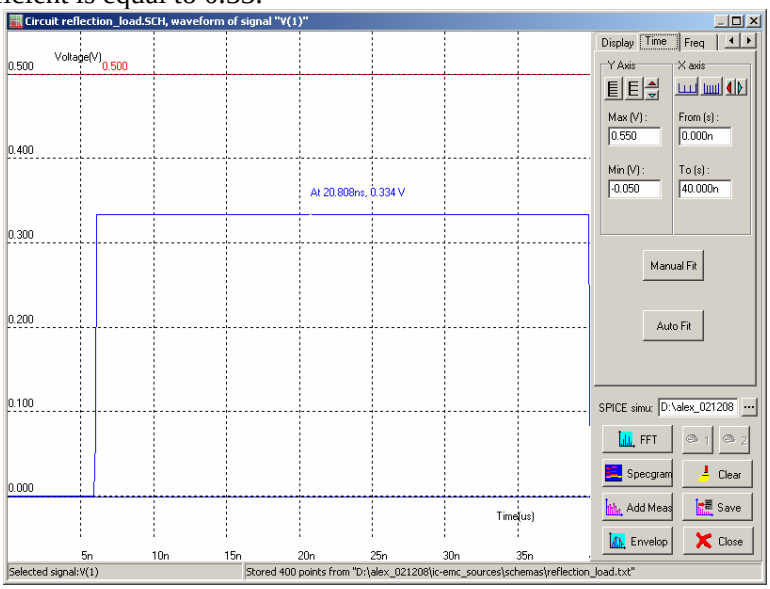


Figure 3-41 : Reflection coefficient at the input/output of the TDR (basic\TDR\reflection_load.sch)

3.8.2 TDR on unmatched load and source impedance

The previous case is typical of an EMC test bench where most of the output impedance and cables are 50-Ω adapted. However, in digital signal design, sources impedances are seldom matched to line characteristic impedance, except in high speed design when mismatch can jeopardize signal integrity and cause bit misrecognitions.

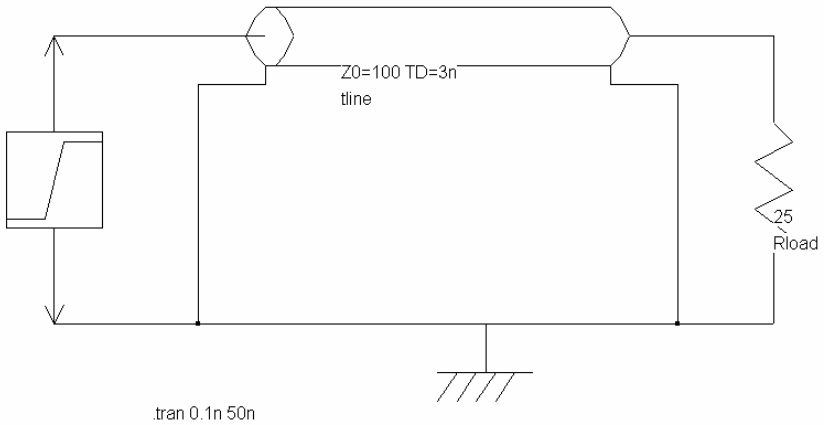


Figure 3-42 : Illustration of the multiple reflections due to double mismatches at source and load impedances (basic\TDR\multiple_reflections.sch)

Let's suppose that the source impedance is different from the line impedance. When the wave reflected by the load termination reaches the source, the source impedance mismatch induces a second reflection and a new wave is reflected from the source to the load. This double mismatch leads to multiple reflections. Therefore, steady-state time takes a much longer time to be reached.
To illustrate the multiple reflection effects, open the file called "basic\TDR\multiple_reflections.sch" (Fig. 3-43). The TDR impedance is equal to 50 Ω, while the line impedance is equal to 100 Ω and the load impedance to 25 Ω. Figure 3-43 presents the simulation results of forward and reflected voltage, figure 3-44 presents the result of the TDR input voltage waveform. At each reflection at the TDR

input/output (every 6 ns), the amplitude voltage waveform is modified.

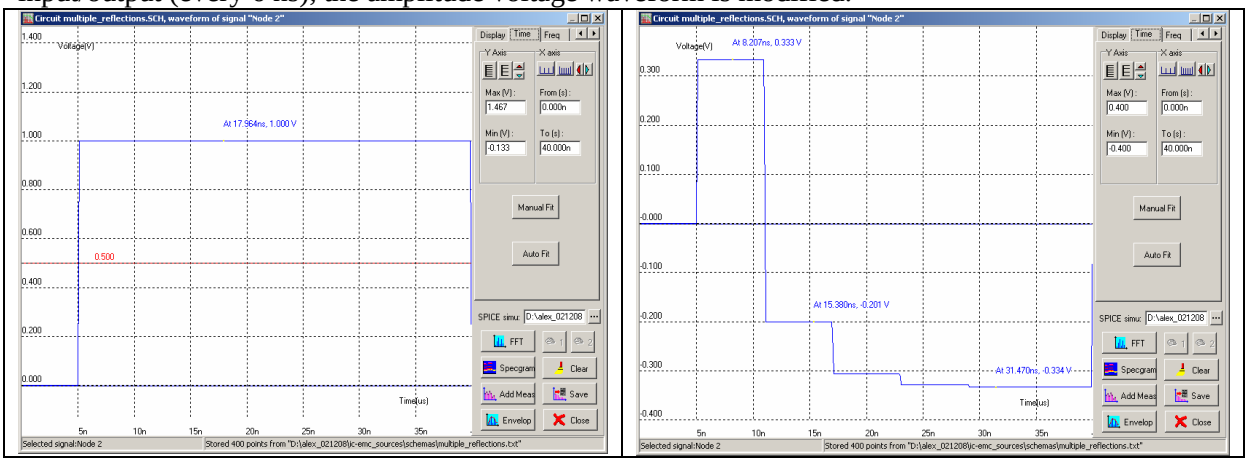


Figure 3-43 : Simulation of the forward (on the left) and reflected voltage (on the right) (basic\TDR_multiple_reflections.sch)

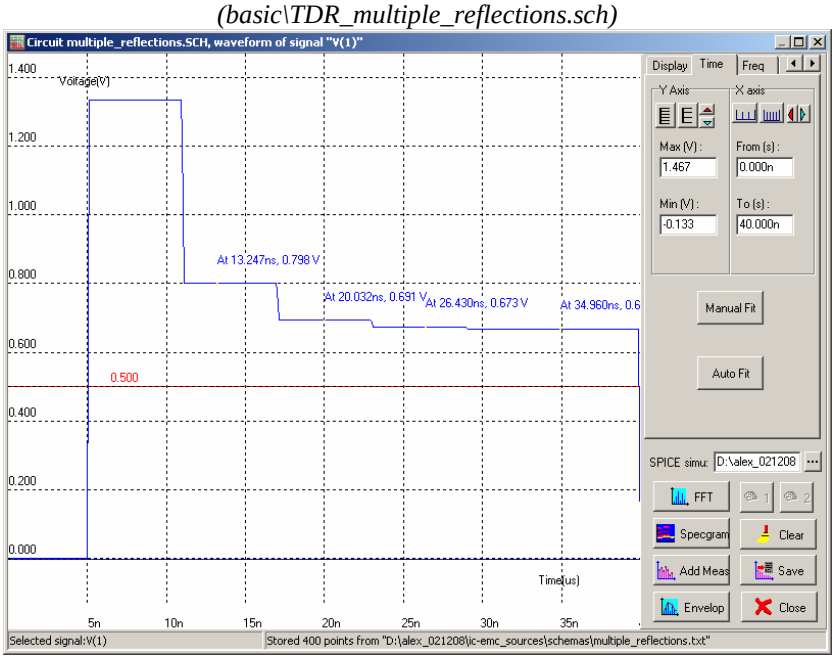


Figure 3-44 : Simulation of the waveform at the input/output of the TDR when multiple reflections occur at the input and output of the line (basic\TDR\multiple_reflections.sch)

Amplitude of the multiple reflections tends to decrease with time since a part of the energy is absorbed by the source and load resistance at each reflection. Amplitude of the voltage waveform tends to 0.66 V. Amplitude of the voltage waveform can be deduced by a bounce diagram, as shown in figure 3-45. Time scale starts with the pulse. V_0 is the amplitude given to the TDR internal voltage generator. The voltage amplitude property given by the user corresponds to the voltage amplitude at the TDR output when the output impedance is equal to the connected load. Therefore, V_0 is equal to two times the voltage amplitude property given by the user. Γ_S is the reflection coefficient of the source; Γ_L is the reflection coefficient of the load. Their amplitudes are given by following equations.

$$\Gamma_S = \frac{Z_S - Z_C}{Z_S + Z_C} = \frac{50 - 100}{50 + 100} = -0.33$$

$$\Gamma_S = \frac{Z_L - Z_C}{Z_L + Z_C} = \frac{25 - 100}{25 + 100} = -0.6$$

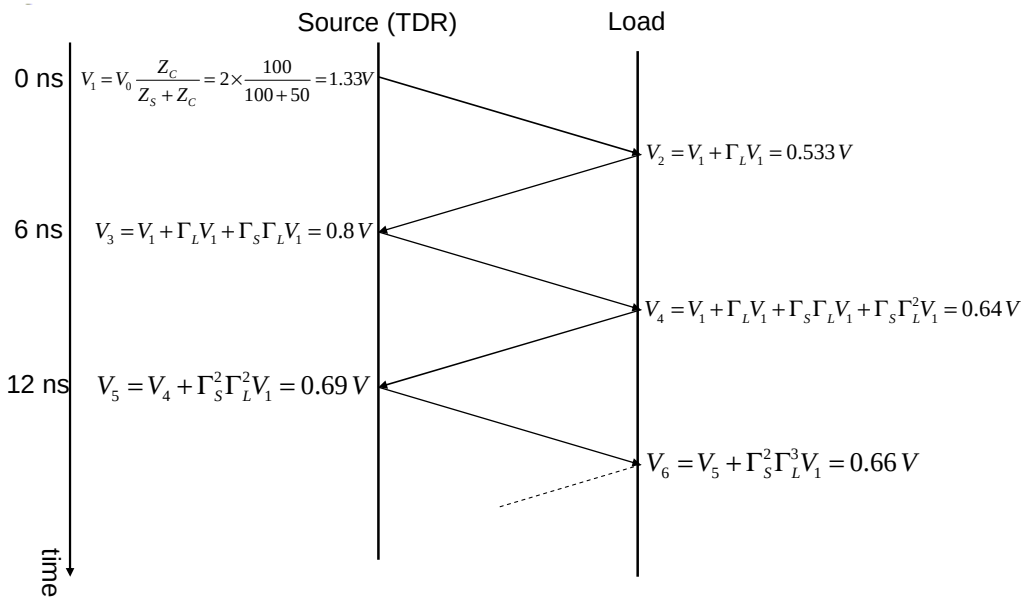


Figure 3-45 : Bounce diagram for the case study described in multiple_reflections.sch

3.9 S parameters

3.9.1 S parameter definition

As explained in the previous sections, impedance mismatches influences power reflections and transfers at each node of a device. These reflections and transmissions define completely the signal propagation characteristics. Scattering parameters (S parameters) are used to represent the reflection and the transfer functions at and between each terminal the device. Measurements of S parameters, generally performed by a vector network analyzer (VNA) are fundamental to extract RF models of components. Figure 3-46 presents a representation of a 2 port device based on a quadripole characterized by S parameters. Ports composed of small signal sinusoidal source and reference impedance Z_0 are connected to device terminals.

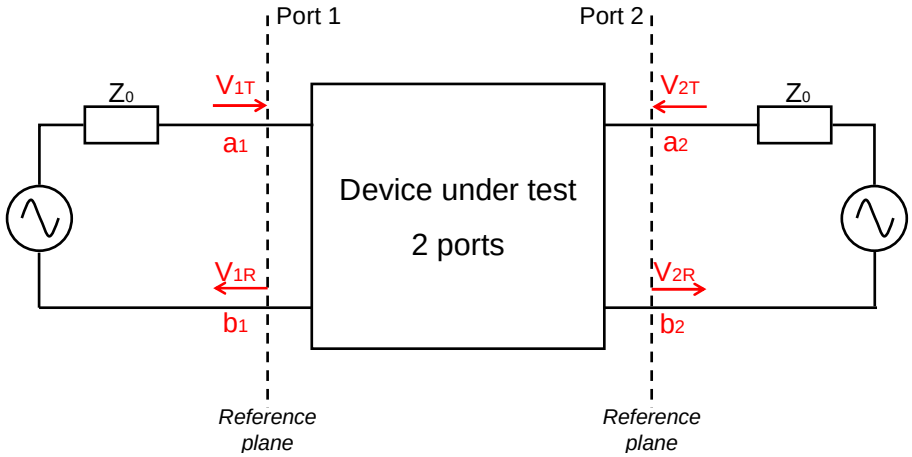


Figure 3-46 : Quadripole representation of a 2 port device

S parameters make a relationship between the forward and reflected power waves at each port of the device under test. Power waves depend on transmitted and reflected voltage at each port and the reference impedance as presented in equations 3-23 and 3-24. Four parameters, listed in table 3-1, allow a complete characterization of power exchanges between the 2 ports. They form the S parameter matrix.

$$a_i = \frac{V_{iT}}{\sqrt{Z_0}} \qquad \textit{Equ. 3-23}$$

$$b_i = \frac{V_{iR}}{\sqrt{Z_0}} \qquad \textit{Equ. 3-24}$$

Input reflection coefficient	**Output reflection coefficient**
$S_{11} = \left.\frac{b_1}{a_1}\right\|_{a_2=0}$ No power fed from port 2. Port 2 terminated by Z0 to prevent from reflection at port 2.	$S_{22} = \left.\frac{b_2}{a_2}\right\|_{a_1=0}$ No power fed from port 1. Port 1 terminated by Z0 to prevent from reflection at port 1.
Forward transmission coefficient	**Forward transmission coefficient**
$S_{21} = \left.\frac{b_2}{a_1}\right\|_{a_2=0}$ No power fed from port 2. Port 2 terminated by Z0 to prevent from reflection at port 2.	$S_{12} = \left.\frac{b_1}{a_2}\right\|_{a_1=0}$ No power fed from port 1. Port 1 terminated by Z0 to prevent from reflection at port 1.

Table 3-1 : Definition of the S parameters of a 2 port device

It can be noted that the input reflection coefficient S11 and S22 are equal to reflection coefficient Γ described by equation 3-22. S parameters are complex values expressed in frequency domains. Their simulations are based on small signal analysis. This kind of modeling can be generalized for a N-port device.

Quadripoles can also be characterized by other parameters, as impedance, admittance … which create a link between other types of values. Equations 3-25 to 3-28 give the relationship between S parameters and the four Z parameters of the impedance matrix.

$$Z_{11} = Z_0 \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \qquad \textit{Equ. 3-25}$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \qquad \textit{Equ. 3-26}$$

$$Z_{12} = Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \qquad \textit{Equ. 3-27}$$

$$Z_{11} = Z_0 \frac{(1+S_{22})(1-S_{11})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \qquad \textit{Equ. 3-28}$$

3.9.2 Passive device S-parameter simulation

IC-EMC proposes S parameter simulation on a N port circuit and a dedicate screen to display simulation results and measurements. To present the S parameter simulation flow, we start with a S11 simulation on a resistive load. Open the file "basic\S_parameters\S11_Rmetal330.sch" (Fig. 3-47). The model consists in a 330 Ω resistive load connected to a S parameter port. The S parameter port symbol is available from the symbol palette  . As the S parameters suppose a small signal analysis, an AC analysis is configured. Double-click inside the S parameter symbol. The interface presented in figure 3-50 opens. The port is characterized by a number, characteristic impedance *Z0* and a DC voltage superposed to the sinusoidal voltage generated by the port. If the box "Enable Port" is checked, the port is included in the simulation, otherwise the port is replaced by a simple resistor with value *Z0*.

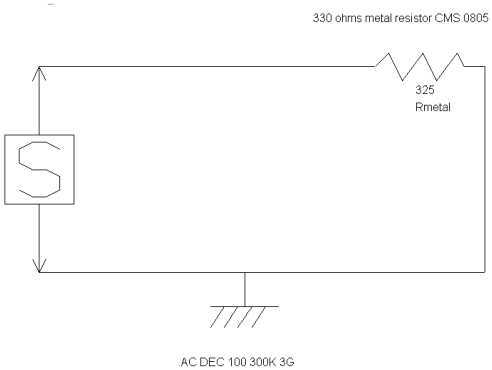


Figure 3-47 : Input reflection coefficient simulation of a resistive load (basic\ S_parameters\ S11_Rmetal330.sch)

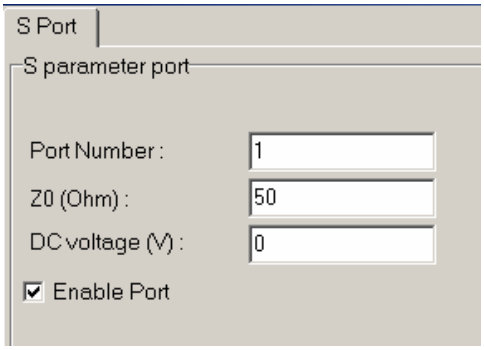


Figure 3-48 : S port symbol properties

The following lines describe the SPICE commands used to simulate the input reflection coefficient. The first lines are linked to the definition of the port, which consists in an AC voltage source and a serial resistor. The last lines define the relations used to compute the S11 parameter. Magnitude and phase of S parameters are computed and printed in the output file in a two-column text format.

```
**** PORT 1 ************************
VPORT1 0 2 DC 0 AC 0
RPORT1 2 1 50
…
AC DEC 100 1MEG 1G
plot mag((V(1)-50*I(VPORT1))/(V(1)+50*I(VPORT1)))
print mag((V(1)-50*I(VPORT1))/(V(1)+50*I(VPORT1))) 180/pi*phase(1e-9+(V(1)-
50*I(VPORT1))/(V(1)+50*I(VPORT1))) >S11_S11_Rload.txt
```

Launch the SPICE simulation and open the S parameter interface at the end of the SPICE simulation by clicking in *EMC → S parameters* or click on the icon  . The new screen appears. The name of the S parameter simulation result file (basic\S_parameters\S11_Rmetal330.spc) should be written in the field *Simulation Data Source*. The computed S parameters and the different proposed associated values are listed respectively in the box “S parameter” and “Value”. Two different display types are proposed: plot the S parameters in a Cartesian graph or in a Smith chart. Keep the default parameters (Cartesian Graph) and click the button *Add*. The plot presented in figure 3-49 appears. The S11 value is constant over all the frequency range and is equal to 0.733.

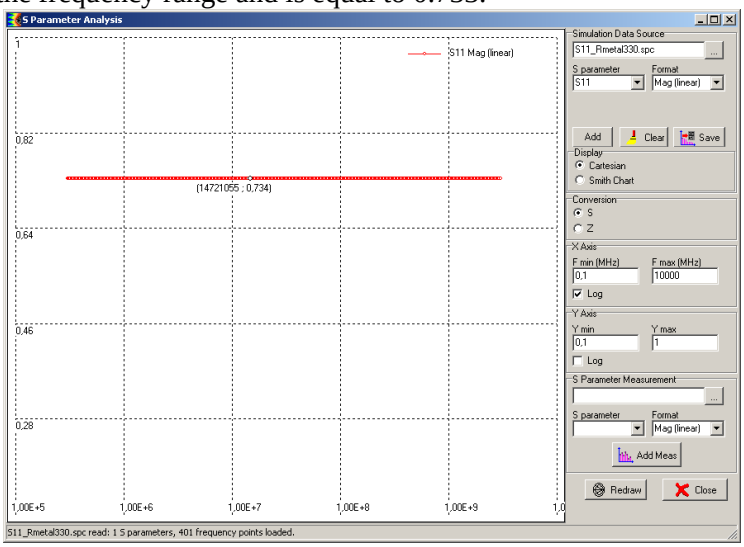


Figure 3-49 : Simulation of the input reflection coefficient of a 330 Ω load (basic\S_parameters\ S11_Rmetal330.txt)

Theoretically, the input reflection coefficient S11 can be evaluated by equation 3-22. For a 330 Ω, S11 is equal to:

$$S_{11}(330\,\Omega) = \Gamma(330\,\Omega) = \frac{330-50}{330+50} = 0.737$$

From the S11 simulation, the input impedance seen from the port can be computed. Select the item "Z" in the sub-menu "Conversion". The plot presented in figure 3-50 appears. The impedance is constant over all the frequency band and equal to 330 Ω. This result is similar to the one that the Z probe would give.

As mentioned in 3.3, ideal models of components are not realistic in high frequency. A CMS metal 330 Ω resistor has been characterized by a vector network analyzer. Click on the button "Add Meas" to load the measurement file. Choose the file called "basic\S_parameters\Meas_S11_R_330ohms.s1p". The file is in the Touchstone format, detailed in annex 12.5. Comparisons between ideal and real-case impedance of the 330 Ω resistor are also given in Fig. 3-50. The impedance is constant up to 300 MHz and, then, tends to decrease due to the parallel parasitic capacitance of the resistor. The capacitance influence is clearly visible in Smith chart format.

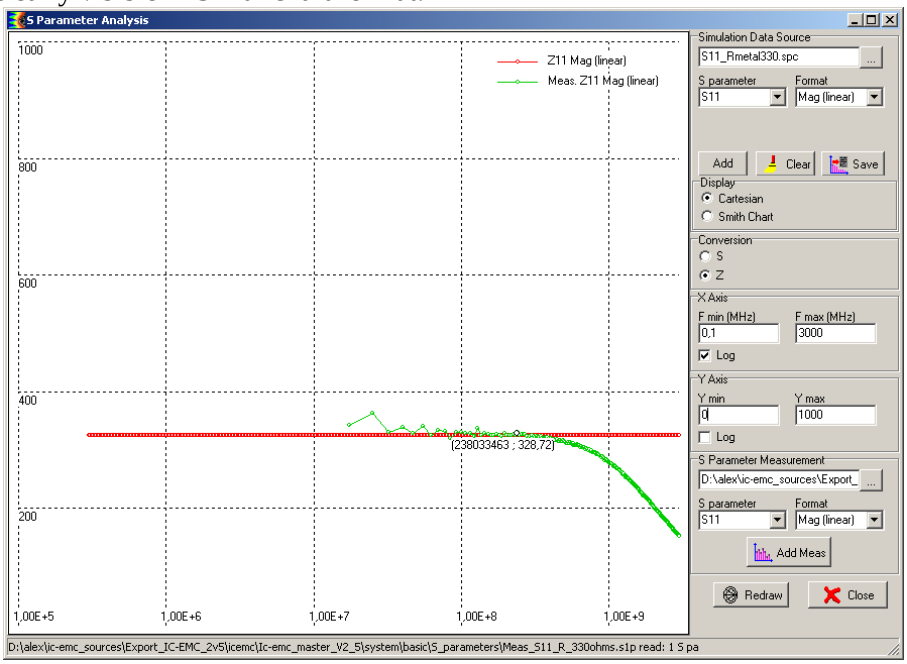


Figure 3-50 : Extraction of the load impedance from the simulated input reflection coefficient (S11_Rmetal330.txt) and comparison with real-case 330 Ω resistor measurements (Meas_S11_R_330ohms.s1p)

3.9.3 N port S-parameter simulation

IC-EMC can address S parameter analysis with N ports. Open the file called "Basic\interconnects\CoupledInterconnectsSparam.sch" (Fig. 3-51). The schematic diagram reuses the example of two coupled interconnects presented in 3.3.1.5. Four ports are placed on each termination of two close 10 mm long interconnects. The model of both interconnects was built from the tool "Interconnect Parameters" and it is valid up to 2 GHz. The numbers of the ports are reported in the figure 3-51.

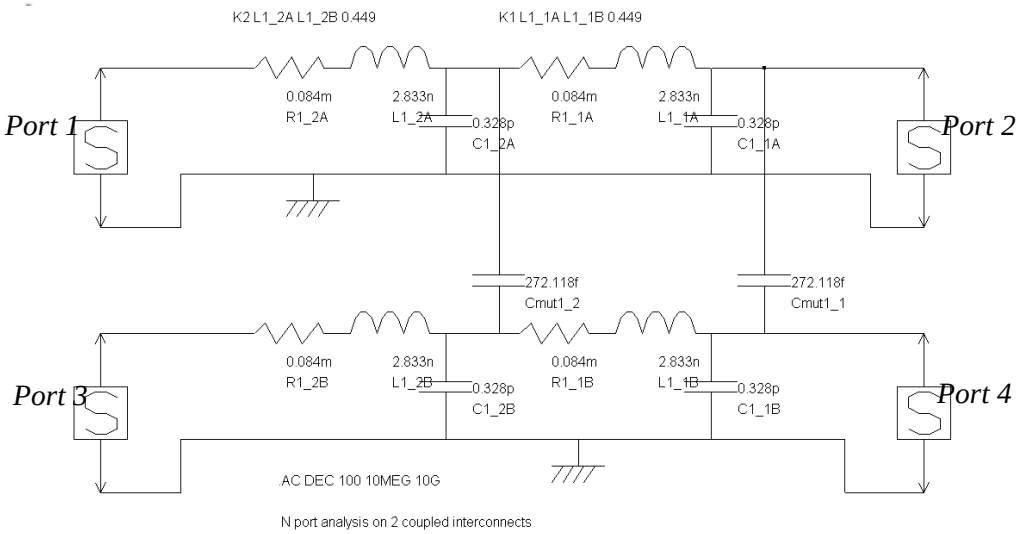


Figure 3-51 : 4 port analysis of two coupled interconnects (Basic\interconnects\CoupledInterconnectsSparam.sch)

Launch the WinSPICE simulation and click in *EMC → S parameters* or click on the icon  to view the simulation result. The result file name "*CoupledInterconnectsSparam.spc*" should appear in the field "Simulation Data Source". In Format, select "Mag (dB)", select the parameter that you want to display in the box "S parameter" and finally click on the button "Add" to display the S parameter curves. Figure 3-54 presents the simulated S11, S12, S13 and S14. S11 and S12 results show that the interconnects transmit efficiently a forward signal. However, reflection losses increase with frequency because the line is unmatched and its length becomes not negligible at high frequency. The parameters S13 and S14 increase steadily with frequency up to 2 GHz. It confirms that the crosstalk has a major impact at high frequency.

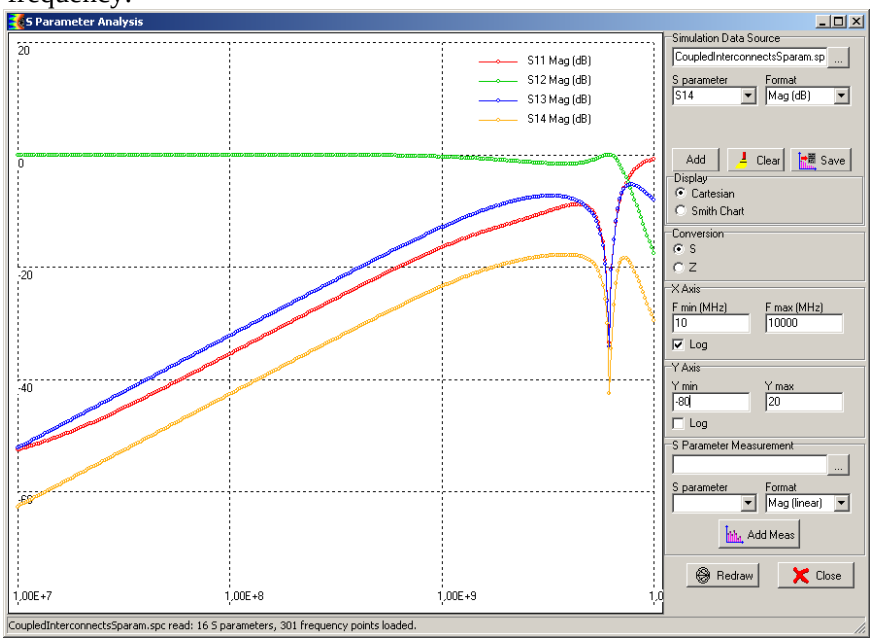


Figure 3-52 : 4 port analysis results of two coupled interconnects (Basic\interconnects\CoupledInterconnectsSparam.spc)

A resonance appears at 3.8 GHz and the transmission coefficient S12 seems to fall above 7 GHz. However, the model is unable to predict correctly the behavior of the interconnect above 2 GHz. Theoretically, the resonance should appear at a frequency such as the wavelength λ and the length l of the interconnect are linked by the following equation:

$$l = \frac{\lambda}{4}, \text{ where } \lambda = \frac{c}{\sqrt{\varepsilon_r}\, f} \qquad \text{Equ. 3-29}$$

From the physical parameters of the line, the resonance frequency is equal to 3.54 GHz. This frequency does not belong to the validity range so that our electrical model can not represent the resonance correctly. A new model with more RLC can be built to solve this limitation. Open the tool "Interconnect Parameters", use the geometrical parameters given in 3.3.1.5, change the limit of validity to 10 GHz and regenerate the model. The SPICE model for S parameter simulation is given in "Basic/interconnects/ CoupledInterconnects10GhzSparam.sch" (Fig. 3-53). Eight RLC cells are used to model the interconnects. Each of them represents a 1.25 mm long piece of the interconnects, so that the λ/10 criterion is valid up to 11.3 GHz.

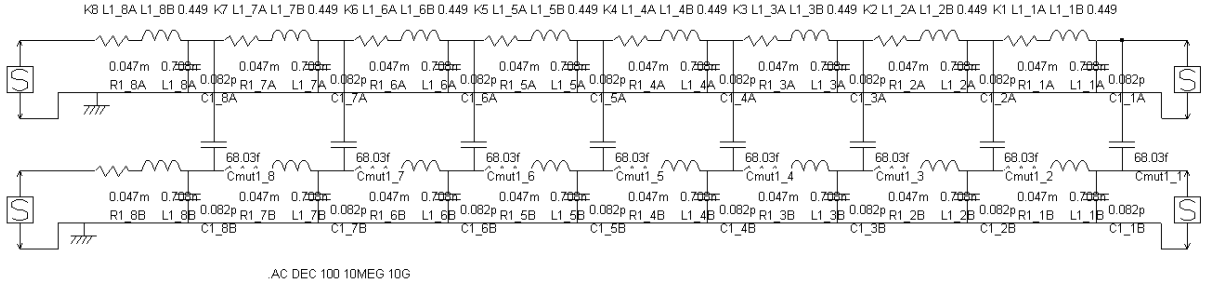


Figure 3-53 : High frequency model of two coupled interconnects for 4 port analysis (Basic\interconnects\CoupledInterconnects10GhzSparam.sch)

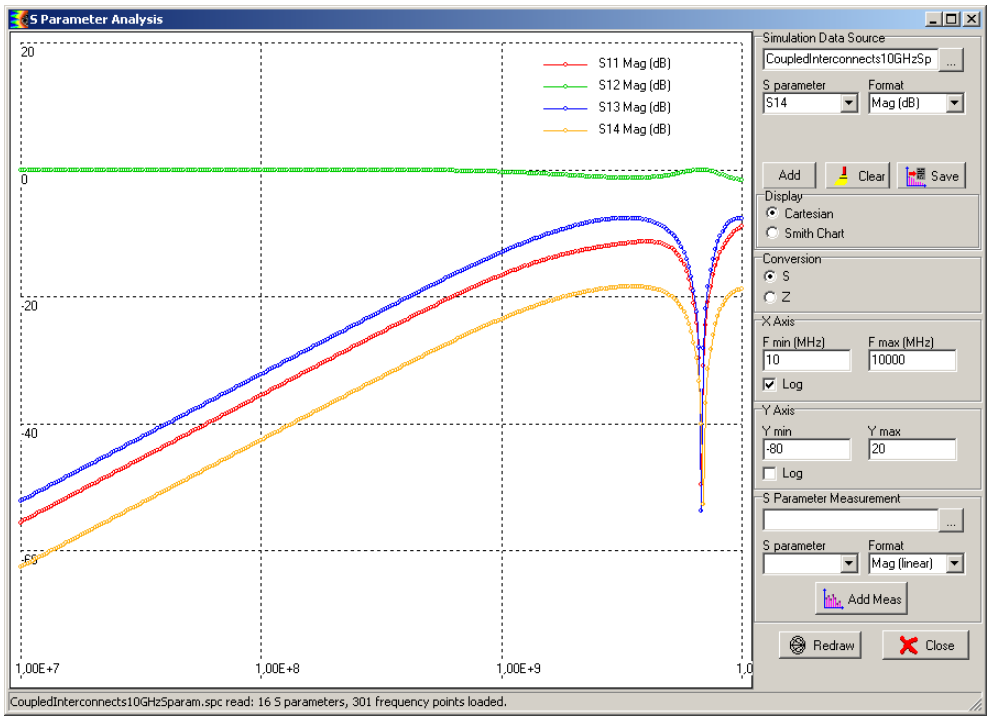


Figure 3-54 : 4 port analysis results of two coupled interconnects valid up to 10 GHz (Basic/interconnects/CoupledInterconnects10GhzSparam.spc)

Figure 3-54 presents the simulated S11, S12, S13 and S14. The results are similar to the previous one up to 2 GHz. The resonance frequency of the interconnects is about 3.5 GHz which correlates with the theoretical value. The transmission through the line remains quite constant over all the frequency range. This model is valid only if dielectric losses are supposed negligible, which is not certainly true.

3.10 Summary

In this chapter, most of the main basic concepts for EMC have been presented. The dB-based units are very useful for comparing signals with large amplitude differences. The Fast Fourier Transform which computes the frequency domain response of a transient signal has also been presented with several classical "tricks". The description of the "Interconnect Parameters" has put the emphasis on electrical parasitic elements of interconnects. Their evaluation is of utmost importance to analyze EMC problems. The representation of impedance in frequency domain has also been illustrated, with a description of the specific screen proposed in IC-EMC to help building equivalent models. This tool is very useful to model accurately and efficiently the behavior of electronic circuits. The effects of unmatched source impedance, characteristic impedance of interconnects and load impedance have been described: analytical formulations, appearance of reflected waves, power matching conditions, impedance matching conditions, degradation of signal integrity… The distortions of signal due to non matching conditions can worsen EMC problems. Finally, the representation of electronic devices by quadripoles and the characterization by S parameters have been presented.

3.11 References

[3-1] Agilent Application Note 243, "The Fundamentals of Signal Analysis", you can download the document at http://cp.literature.agilent.com/litweb/pdf/5952-8898E.pdf.

[3-2] C. R. Paul, "Introduction to Electromagnetic Compatibility", Wiley InterScience, 1992, ISBN 0-471-54927-4

[3-3] C. Christopoulos, "Principles and Techniques of Electromagnetic Compatibility", CRC Press, 1995, ISBN 0-8493-7892-3

[3-4] M. I. Montrose, "Printed Circuit Board Design Techniques for EMC Compliance", IEEE Press, 1996, ISBN 0-7803-1131-0

3.12 Exercises

5. Exercise 1 – Fast Fourier transform of a trapezoidal signal

Simulate the FFT of the following signals and comment the results.

- 50 % duty cycle trapezoidal signal: V0 = 0V, V1 = 5 V, Tr = Tf = 1 ns, PW = 49 ns, Period = 100ns
- 10 % duty cycle trapezoidal signal: V0 = 0V, V1 = 5 V, Tr = Tf = 1 ns, PW = 9 ns, Period = 100ns.

6. Exercise 2 – Aliasing

Open the file "Basic/FFT/FFT_sinus.sch" and save the file as "Aliasing_Illustration.sch". The schematic contains a sinus waveform voltage generator loaded by a 50 Ω load. The frequency of the signal is 100 MHz. Modify the transient simulation characteristics and set the sampling period to 15 ns. Simulate with WinSPICE and plot the FFT response of the signal delivered by the voltage source. Comment the result.

7. Exercise 3 – Decoupling capacitor and target impedance

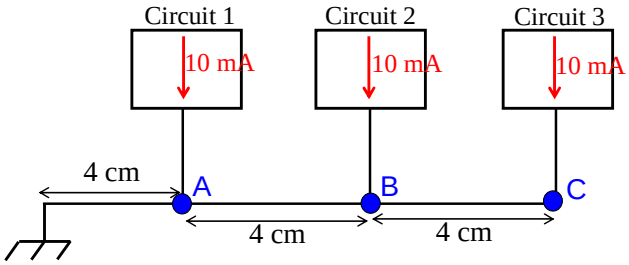
A 4.7 nF ceramic capacitor has two copper leads (σ = 5.8e7 S/m) of length 1 cm and diameter 0.25 mm.

1. Plot the capacitor impedance as a function of frequency from 10 kHz to 1 GHz.
2. This capacitor is used to decouple a circuit. This circuit is supplied under 2.5 V and

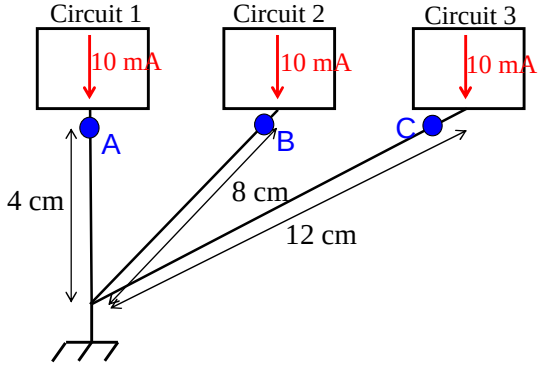
consumes a current of 1 A. The specification in term of maximum ripple voltage is set at 10 % of the power supply voltage. Determine the frequency range over which the capacitor is effective as a decoupling capacitor?

8. Exercise 4 – Grounding strategy

Three circuits are connected to ground at a common point using the two schemes shown below. Assume that each of these 3 circuits draws a current of 1 mA at 100 MHz. Ground connections are ensured by 2 mm wide and 35 µm thick copper tracks, made on a 1.6 mm thick FR4 substrate. Determine the amplitude of parasitic voltage generated at points A, B and C for these two grounding techniques. Which is the most effective in terms of noise reduction?



Grounding technique 1



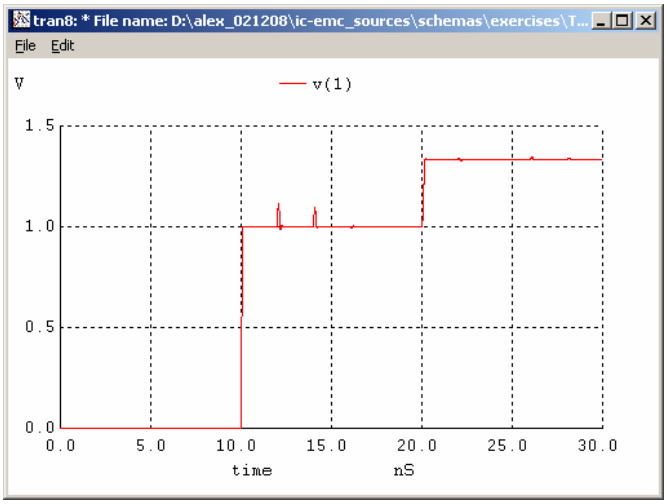
Grounding technique 2

9. Exercise 5: Impedance model extraction:

The impedance of two ceramic capacitors has been measured with a vector network analyzer. The measurement results are available in the file "basic\impedance\ Zin_Capa4v7uCeram.z" and "basic\impedance\ Zin_Capa47pCeram.z". What is the nature of this passive device? Propose electrical models for these passive devices.

10. Exercise 6: TDR analysis of a PCB track

Let's consider a track designed on a FR4 board. The track starts from a connector placed on the top side of the board, passes on the bottom side and finally connects a load placed on the top side. Two via are used to connect both faces. The following figure presents the TDR measurement performed from the connector. The characteristic impedance of the TDR is 50 Ω.



1. Deduce from the waveform the distance between the input of the line and the vias, and the distance between both vias.

2. What is the impedance of the line termination?

11. Exercise 7: Termination matching

The output buffer of a CMOS circuit is connected to the input buffer of another CMOS circuit, through a printed circuit board track. The output buffer is supposed ideal; its output impedance is matched to the PCB track. The output buffer generates a 50 MHz trapezoidal signal with a 2 ns rise/fall time. The input buffer is modeled by a 6 pF capacitance. The characteristics of the line are:

- Length = 10 cm
- Width = 0.508 mm
- Thickness of the board = 1.6 mm
- PCB material = FR4 (ε_r = 4.6)

1. Build an electrical model of the PCB track and connect the model of the output and input buffer. Simulate the transient signal at both terminations of the PCB tracks. What do you observe?

2. Simulate the reflection coefficient seen from the output buffer. What can you conclude?

3. Add a parallel resistor the load and choose an adequate value. What is the impact on the coefficient reflection?

4. Simulate for both terminations the voltage waveform at buffer outputs. Analyze the voltage waveform.

12. Exercise 8: Line loaded by a capacitance

CMOS Circuit inputs are capacitive. When a CMOS output buffer is connected to a CMOS input buffer by a PCB line, the equivalent capacitance of the input buffer tends to slow the propagation through the line and reduce the characteristic impedance of the line. For high speed digital design, this effect can have dramatic consequences for signal integrity because of large ringing. This exercise aims at finding rules to avoid signal transmission issues and applying them on an ideal case.

Let's consider I/O buffer supplied under 2.5 V connected by a PCB line with the following characteristics:

- track width = 0.508 mm
- track length = 2 cm

- substrate height = 1.6 mm
- substrate FR4

1. With the tool Interconnect Parameters, compute the characteristic impedance and the lineic inductance and capacitance of the line. Compute the propagation delay per length unit T_{PD} in the line.

2. A capacitive load Cd is connected at the end of the line. Let's suppose that this load is distributed along the line. Compute the characteristic impedance Z_0'and the propagation delay per length unit T_{PD}' for the loaded line. Conclude about the effect of the capacitive load on the characteristic impedance and the propagation delay.

3. Open the file "basic\interconnects\loaded_line.sch". The output buffer is modeled by a TDR generator with a rising time of 500 ps and an internal serial resistor of 10 ohms. The input buffer is modeled by a 10 pF capacitor. The PCB line is modeled by an ideal transmission line. Enter the parameter of the transmission line and simulate the voltage waveform at each terminations of the transmission line for a 0.1 pF load capacitor (equivalent to an unloaded line) and a 10 pF load capacitor. Explain the difference observed in both simulations.

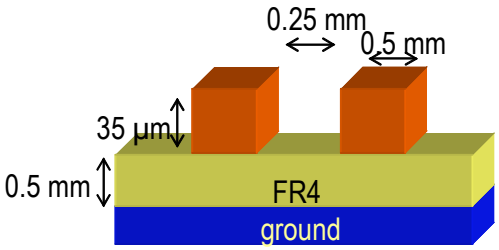
4. Propose a relation between the propagation delay and the rise or fall time of the forward voltage to prevent signal integrity issues. Formulate two rules concerning the rise/fall time of the forward signal and the line length.

5. Modify the schematic "basic\interconnects\loaded_line.sch" to reduce ringing appearing at voltage step. (Modify the rise time of the TDR generator and the line length). Find the rise time and the line length to reduce the amplitude of the overshoot under 20 % of the power supply.

6. Reinitialize the values of rise time and line length. Compute the characteristic impedance of the loaded line. Add a serial resistor at the output buffer and observe the effect on the waveform at each terminals of the load. A practical value for the resistor is the characteristic impedance of the loaded line. What do you think about this rule?

13. Exercise 9: Crosstalk

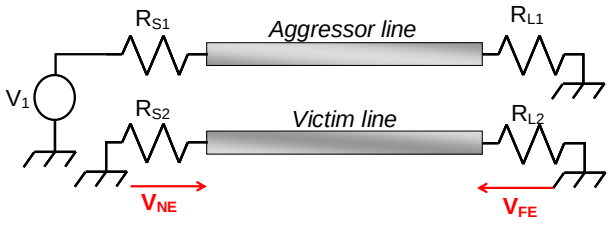
Two nearby microstrip lines are drawn on a 1.6 mm thick FR4 printed circuit board (εr = 4.5). The lines are 0.5 mm wide, 35 µm thick and 1 cm long, and separated by a 0.25 mm gap. One line is supplied by a voltage generator and is called the aggressor line, while the second is not supplied and is called the victim line. This exercise aimed at computing the maximum amplitude of the noise coupled on the victim line due to crosstalk.



1. Compute the lineic electrical parameters of these coupled lines.

2. A square signal is applied at one termination of one of the line. Its characteristics are:

- Vmin = 0 V, Vmax = 5 V
- Period = 100 ns, duty cycle = 50 %
- Rising and fall time = 2 ns



The other terminations are loaded by 50 ohms. VFE and VNE are the far end and near end

voltages. How many RLC cells should be placed in the mode to satisfy the quasi-static approximation over all the bandwidth of the signal? Propose an equivalent electrical schematic of these coupled lines.

3. From the complete electrical model, propose an equivalent model for the victim line. Deduce literal expressions of far end and near end peak voltage on the victim line.

4. Verify the validity of the formulation in simulation.

5. Do you think that the near and far end voltage induced by crosstalk can induce EMC issues?

6. Are the previous formulations still valid for a 10 cm line?

4 The IBIS Standard and its use in EMC of ICs

IBIS (Input/Output Buffer Information Specification) [4-1] is a standardized format for analog interfaces of digital I/O buffers modeling. IBIS is very popular because it provides the right balance between comprehensive detail of the IC and sufficient accuracy for signal integrity simulation [4-2]. In EMC analysis at IC level, IBIS models enable reasonably accurate and fast IO switching simulations. However, IBIS models do not include core noise information. We describe here how to exploit the IBIS information and apply it to EMC simulation at IC level [4-3].

4.1 Introduction to IBIS format

An IBIS model is formatted as human-readable ASCII text. It is mostly based on extracted tables of generic structural elements. IBIS models are *component-centric*; the IBIS model describes all pins of the physical component with an associated model. Keywords are denoted by square brackets, and a vertical bar serves as the default comment character. The IBIS file mainly contains the following elements:

- **Information and Specification** content starting with a header block [IBIS Ver] and also presented elsewhere throughout the file
- **Package** information within each of one or more [Component] blocks and under a default [Package] keyword
- **Pin out** information within each of one or more [Component] blocks and under the [Pin] keyword giving pin-specific model references and optional pin-specific package values
- **Model** blocks beginning with one or more [Model] keywords.

The software IC-EMC is able to extract RLC information from IBIS files in a simple way. Using the command **File → Load Ibis File**, and selecting the IBIS file "IBIS/s12x_v2.ibs"), the following screen appears (Figure 4-1).

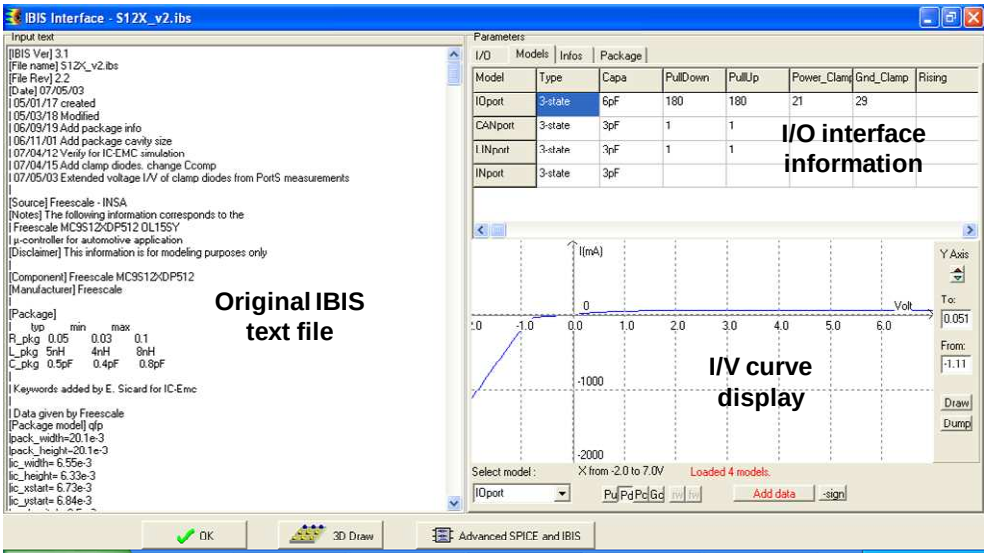


Figure 4-1: Loading an IBIS file in IC-EMC (ibis\s12x_v2.ibs)

The [Model] block contains the data for electrical simulation of the pin interface. The Model_type sub-parameter classifies the model by types including Input, Output, I/O, 3-state, etc. Static I-V table blocks documented by [Pullup] and [Pulldown] keywords tabulate the transistor drive strengths. In the IBIS window of IC-EMC, the button "Pu" corresponds to pullup, and "Pd" to Pulldown. The diodes

are documented by [Power Clamp] and [Gnd Clamp] I-V tables ("Pc" for Power Clamp, "Gc" for Gnd Clamp). In CMOS technology, clamp diode currents come from P-N junctions. These junctions act as protection circuits from voltage over-stress.
It can be seen from the example shown in figure 4-1 (S12X microcontroller from Freescale) that pull-up, pull-down, power-clamp and gnd-clamp models are available for the IO type "IOPort". The I/V curve provided by the IBIS file is plotted in the right part of Fig. 4-1. In this example, the I/V curve corresponds to the pull-down device.

4.1.1 Convert an input into RLC diagram

Click the desired input pin in the I/O list, then click the button "One pin into RLC". The input pad is converted into a RLC circuit with on-chip capacitance and clamp, as shown in figure 4-2. It consists, from left to right, in an IO symbol with the input name (Here 'PT0'), the R,L,C parameters for the package (Here LPT0,CPT0,RPT0), and the component input capacitance (Ccomp_PT0). Notice the connection to the substrate potential "Vsub".

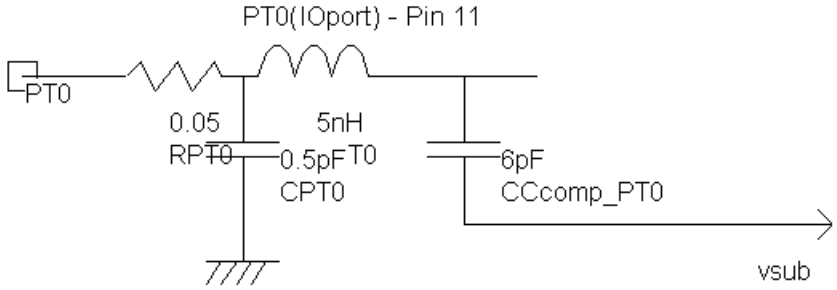


Figure 4-2 : Model of the PT0 pad (ibis\s12x_v2.ibs)

4.1.2 Protection Diode Modeling

The diodes used for Electrostatic discharge (ESD) protections may be added to the schematic diagram by asserting the item "Add Gnd/Power clamps". In Fig. 4-3, we can see the clamp diodes connected to the internal node, and supplied by "VDDIO" for the power clamp and "Vsub" for the GND clamp.
The clamp appearing in the figure should be tuned to fit the I/V characteristics given in the IBIS file. The I/V characteristics may be displayed by a simple click in the "Models" item from the IBIS window, and by selecting the gnd_clamp (GC) or power_clamp (PC) model in the bottom menu, if accessible. If the button is not selected, this means that no data has been provided in the IBIS file for the corresponding I/V curve. The basic diode parameters are listed in Table 4-1.

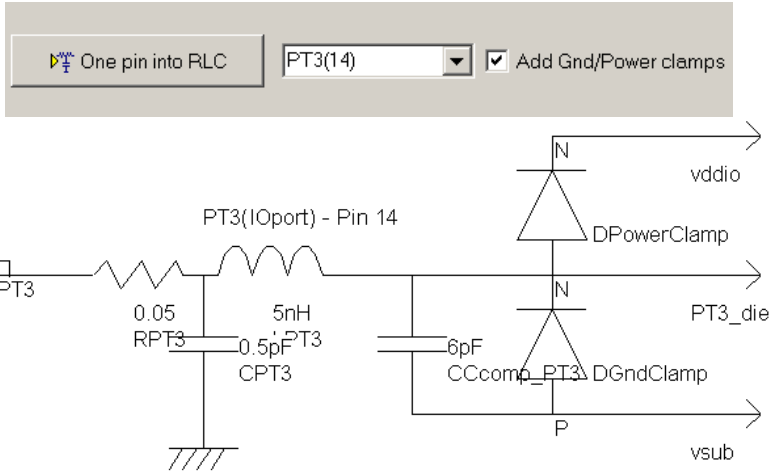
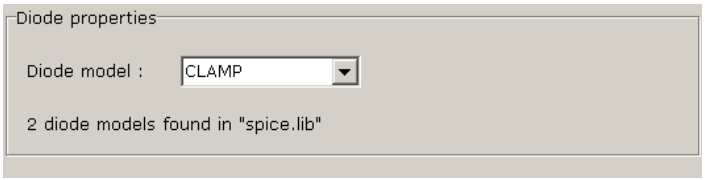


Figure 4-3: From IBIS to an R,L,C, diode network of the PT3 (ibis\s12x_io_pt3.sch)

Parameter	Description	Typical
Is	Saturation current	10^{-14} A

N	Emission coefficient	1
Rs	Ohmic serial resistance	2 ohm
vj	Junction potential	0.7 V
fc	Forward bias junction fit parameter	0.5
Bv	Reverse breakdown voltage	10 V
ibv	Current at reverse breakdown voltage	10^{-3} A

Table 4-1 : Basic diode parameters




```
*---Diodes------------
* Simple diode
.MODEL DIOD D RS=1 BV=10
*
* Clamp diode
.MODEL CLAMP D RS=2 BV=10 N=1.2
```

Figure 4-4: The diode models proposed in the spice library (ibis/spice.lib)

IC-EMC uses the default file “Spice.Lib” for MOS and Diode models, available in System\lib directory. The library includes two diode models, one called “DIOD”, which appears by default, the other called “CLAMP” with slightly different parameters (Fig. 4-4). By default, IC-EMC assigns “CLAMP” models to clamp diodes.

The DC simulation of the S12X input may be performed using the setup proposed in Fig. 4-5. A voltage source is applied to the input. The relevant information is the DC current consumption for an input voltage source ranging from –VDD to +2.VDD. The current consumption versus input voltage can be plotted using the label “.plot –i(Vio)”. The DC simulation is controlled by the label “.dc Vio -5.0 10 0.1”, which means that the voltage supply Vio is swept from -5.0 V to 10.0 V with a 0.1 V step.

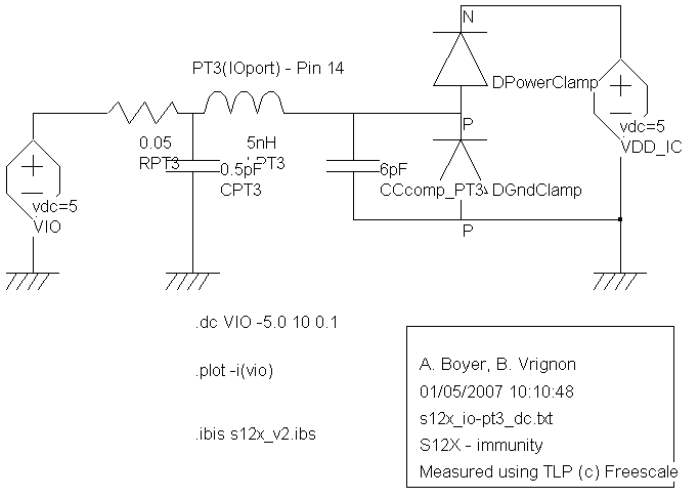


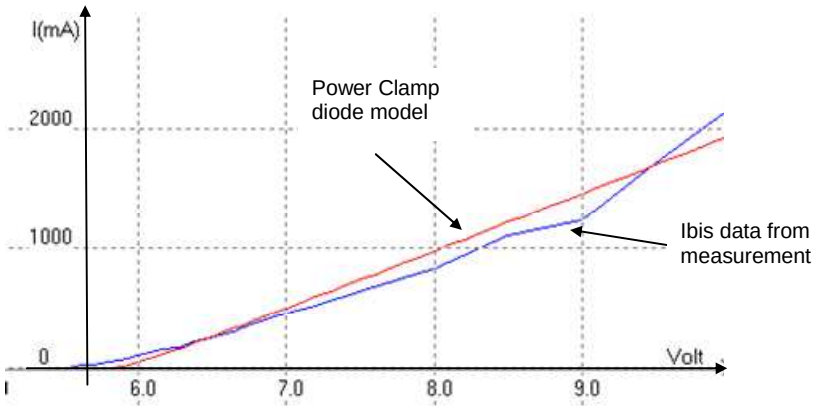
Figure 4-5 : Setup for DC simulation of the IO. The supply range has been extended from –VDD to 2.VDD (ibis/s12x_io_pt3_dc.sch)

The simulated data and the IBIS information may be compared using the following procedure:

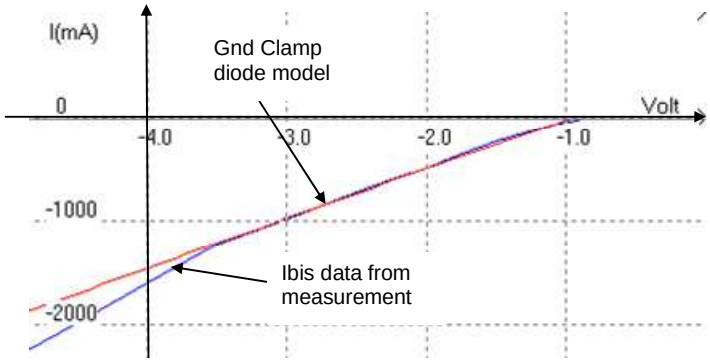
<table>
<tr><td>1. Select the Ibis Window</td><td> 

Click “EMC → Ibis Interface” or click the [ibs] icon.</td><td>The IBIS information related to the S12X component appears.</td></tr>
<tr><td>2. Select the I/V curve of the power clamp</td><td>Click “Models”. In the array, click in the line “I/O Port”, column “Power_clamp”. The I/V of the Power_clamp is shown.
<table>
<tr><th>Model</th><th>Type</th><th>Capa</th><th>PullDown</th><th>PullUp</th><th>Power_Cla</th><th>Gnd_Clam</th></tr>
<tr><td>IOport</td><td>3-state</td><td>6pF</td><td>180</td><td>180</td><td>21</td><td>29</td></tr>
<tr><td>CANport</td><td>3-state</td><td>3pF</td><td>1</td><td>1</td><td></td><td></td></tr>
<tr><td>LINport</td><td>3-state</td><td>3pF</td><td>1</td><td>1</td><td></td><td></td></tr>
<tr><td>INport</td><td>3-state</td><td>3pF</td><td></td><td></td><td></td><td></td></tr>
</table></td><td>Selects the I/V curve in the IBIS file corresponding to the DC diode measurement.</td></tr>
<tr><td>3. Load the I/V simulation of the power clamp</td><td>Click “Add Data” and select the file “s12x_io_pt3_dc.txt”. The simulation result is superimposed to the IBIS information. 

. Screen presented in fig. 4-6 should appear.</td><td>The data sign may be changed by a click on “-sign”.</td></tr>
<tr><td>4. Load the I/V simulation of the gnd clamp</td><td>Click “GC” to superimpose the GND clamp ibis information to the simulation</td><td></td></tr>
</table>



(a) Power clamp simulation and IBIS information



(b) GND clamp simulation and IBIS information

Figure 4-6: Comparing IBIS data and simulation of the power and Gnd clamp diodes (ibis/s12x_io_pt3_dc.sch)

4.1.3 Converting an output

Now, choose the desired output pin in the list and click the button "One pin into RLC". The output pad is modeled by the RLC elements of the package and the on-chip capacitance as for the input pad. One

n-channel MOS device and one p-channel MOS device are added to the schematic diagram to account for the buffer. The width and length of these MOS devices are critical parameters.
The complete circuit is shown on fig. 4-7 and consists, from left to right, to the supplies for the buffers and a voltage source, the buffer and protection diodes, the R,L,C parameters for the package the pad capacitance and a load as a termination.

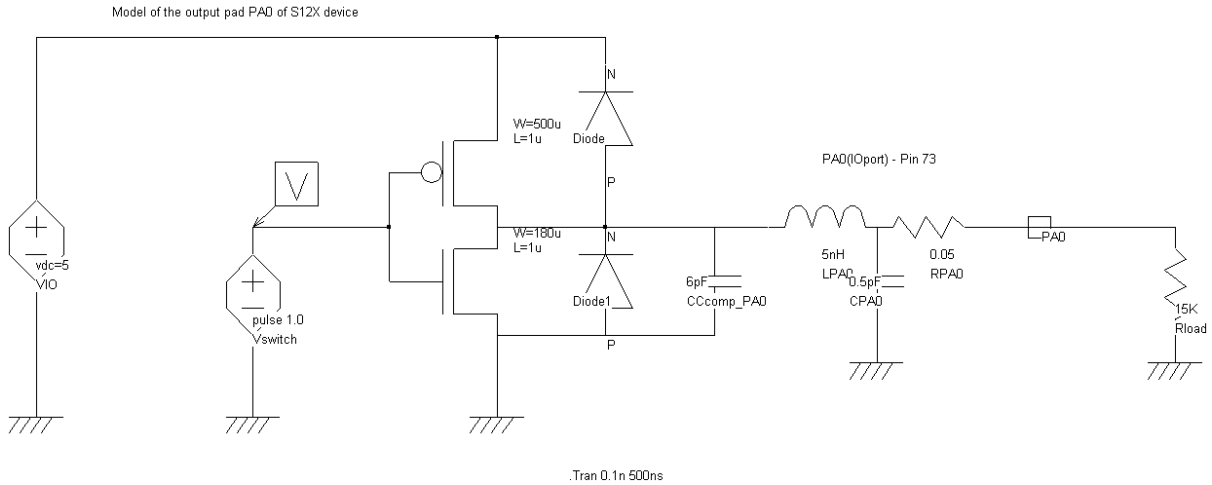


Figure 4-7 : Model of an output pad (ibis/s12x_io_pa0.sch)

4.2 Comparing IBIS and Winspice MOS characteristics

We use the basic MOS model 3 which provides a good compromise between simulation efficiency and accuracy. However, more advanced models such as BSIM4 [4-4] also supported by WinSpice may be used. The basic setup is shown in figure 4-8.

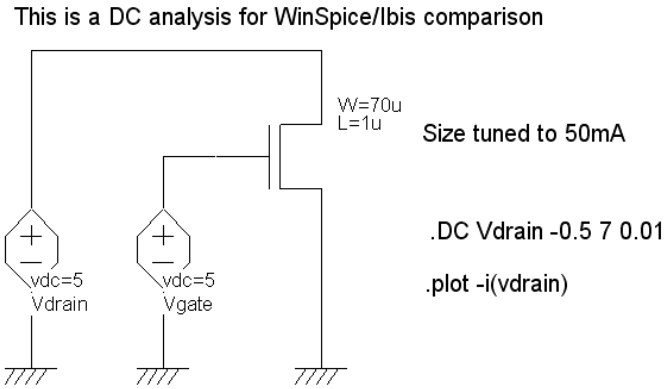


Figure 4-8 : The simulation setup to produce the nMOS i/v characteristics (ibis/nmos_dc.SCH)

The simulated data and the IBIS information may be compared by a click in the button "Add Data" situated on the lower right corner of the window. We choose the WinSpice data file 'nmos_dc.txt' to enable the comparison between the IBIS and spice information. The comparison example is provided in figure 4-9. The main fitting parameter is the MOS width W. The length L is fixed to 1 µm. It is not recommended to change the MOS model parameters without prior information about the technology.

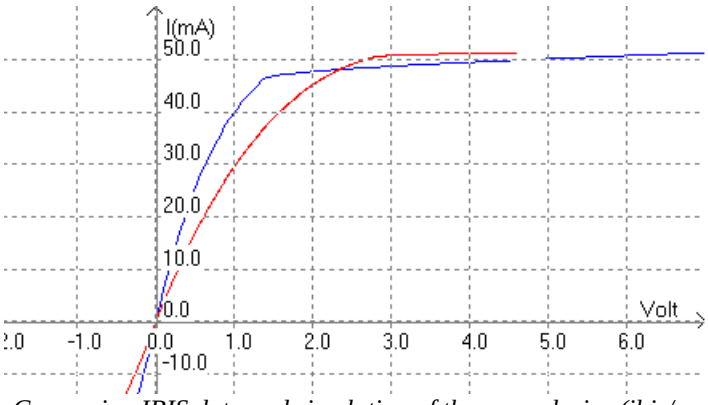


Figure 4-9 : Comparing IBIS data and simulation of the nmos device (ibis/nmos_dc.SCH)

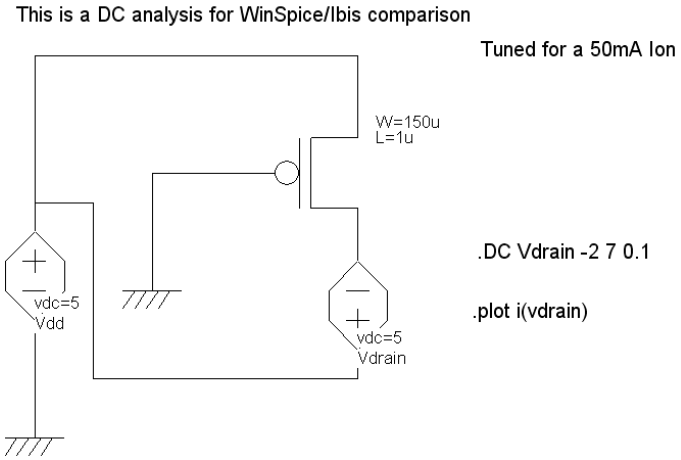


Figure 4-10: Simulation setup for the pmos device (ibis/pmos_dc.SCH)

We perform the same study for the pMOS. The simulation setup is a little tricky as shown in figure 4-10. The simulated data and the IBIS information may be compared by a click in the button "Add Data" situated on the lower right corner of the window (Figure 4-11).

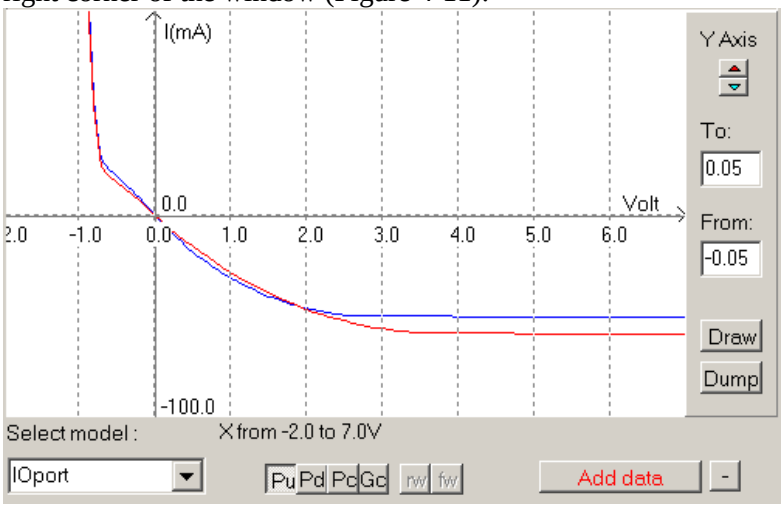


Figure 4-11 : Comparing IBIS data and simulation of the pmos device (ibis/pmos_dc.SCH)

4.3 Package

In most cases, accurate R,L,C evaluation of the package leads and bondings is not available in preliminary IBIS files. The purpose of the 2D and 3D-package reconstruction available in IC-EMC is to ease the extraction of package R,L,C elements and gives precise space localization of the leads, useful for near field radiated emission simulation presented in chapter 6.

4.3.1 Hidden Keywords

Some important information is resourced in the IBIS file related to the package and IC physical dimensions. The information is placed in the [Package model] section, and starts by « | » to avoid parsing errors with conventional IBIS loaders. The physical dimensions are very important information to rebuild the lead frame structure of the package, together with the bonding structure and access to the die. Table 4-2 provides a list of the important hidden parameters and associated description added in IBIS file, and used to configure the package viewer in IC-EMC. Fig. 4-12 illustrates the meaning of these geometrical parameters. The complete list of hidden parameters is given in the reference manual, section "Ibis", (chapter 11.1.9).

Hidden parameter	Description	Example
pack_width	Package width	20.1e-3 m
pack_height	Package height	20.1e-3 m
ic_width	Die witdh	6.55e-3 m
Ic_height	Die height	6.33e-3 m
ic_xstart	Die location in X related to the package	6.73e-3 m
ic_ystart	Die location in Y related to the package	6.84e-3 m
pack_pitch	Package pin pitch	0.5e-3 m
ic_altitude	Die altitude over the ground plane	0.8e-3 m
pack_ball	BGA ball radius	0.25e-6 m

Table 4-2 : Hidden parameters stored in the [package model] section

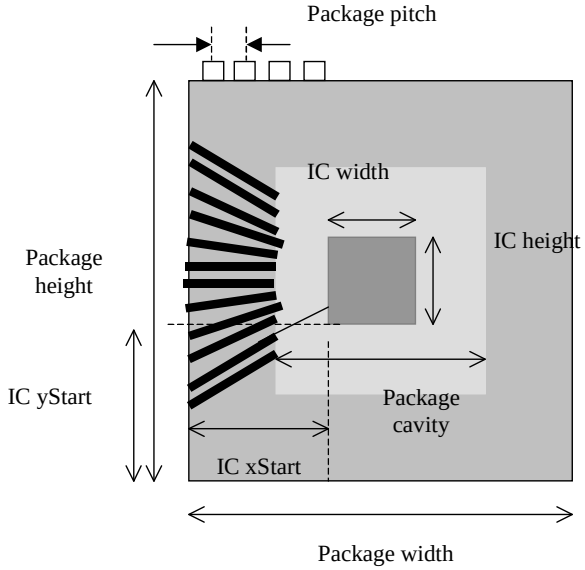


Figure 4-12 : Main parameters required for an estimation of the package R,L,C model

Different package reconstruction methods exist and depend on the package type. The keyword [Package Model] provides information about the package type.

Keyword	Type	IBIS example file
[Package Model] ubga	Micro BGA	infineon_tc1796.ibs
[Package Model] sop	SOP package	ahct04.ibs
[Package Model] qfp	Quad Flat Pack (QFP)	Cesame_v14.ibs S12x_v2.ibs
[Package Model] dil	Dual in line (DIL)	

Table 4-3 : Examples of package declaration in the ibis file

4.3.2 2D Package Viewer

The need for reconstructing the 2D aspect of the package is justified by the need to provide accurate space coordinates for lead and bondings for near-field scan prediction (cf. chapter 6). The external aspect of the IC with pin placement may be displayed by a click on the item "Package" (figure 4-13).

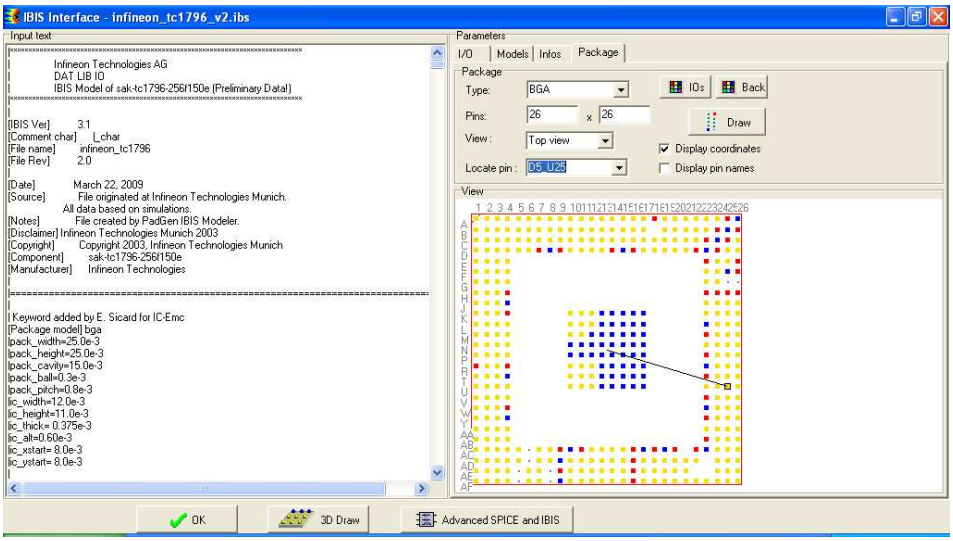


Figure 4-13: Package viewer (case study/tricore/infineon_tc1796_v2.ibs)

The yellow color corresponds to general purpose I/Os, the VDD supply is drawn in red, and the VSS supply in blue. Non-connected pins are drawn in gray. This 2D view gives details on the supply structure. It is also used by IC-EMC to compute the approximate position of a package lead. Considering the pin "D4_V26" selected in the pin list, an [X,Y] position is assigned to the lead which appears as a black line in Fig. 4-13, bottom right. The example concerns a 32-bit microcontroller mounted on a BGA from Infineon (TriCore TC1796).

4.3.3 3D package Viewer

The 3D-viewer is a visual assistant but do not include specific EMC features. The need for reconstructing the 3D aspect of a package is justified by the two following items:

- Compute accurate values for R,L,C of the package based on the physical dimensions of leads and bonding, if not provided in IBIS
- Provide accurate space coordinates for lead and bondings for near-field scan prediction

The 3D package viewer gives a three-dimensional interactive view of the package. An example of 3D view of a BGA package is given in figure 4-14.
You may change the viewer's position thanks to cursors X,Y and Z. The Z cursor serves as a zoom. The light position may be changed. The bonding, upper part of the package and the IC may be removed from the drawing. Finally, you may see a particular pin in the pin list given in the lower corner of the user's menu. The demo button makes an automatic rotation of the object, and the "close" button closes the window.

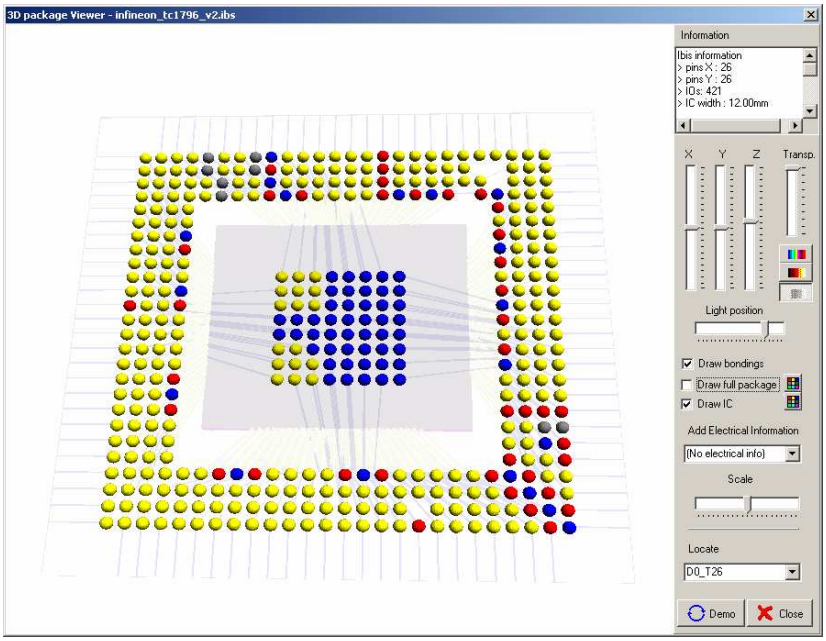


Figure 4-14 : 3D view of a BGA package (case study/tricore/infineon_tc1796_v2.ibs)

4.4 Advanced SPICE and IBIS

The module « Tools → Advanced Spice and IBIS » generates SPICE-compatible and IBIS-compatible netlists including the package parasitic R,L,C values for each package pin. This tool saves the time of tedious data entry required in the more sophisticated three-dimensional programs that require large amounts of CPU time. In appendix H, you could find a more precise method to extract model of package. This section describes the main features of the module.

4.4.1 Principles

The program builds a package layout by using the user-defined dimensions to generate approximate lengths and positions of the package's internal routing. The information required is the package type, pin pitch, pin list, package size and cavity size (Fig. 4-15). The information is listed using hidden keywords added to the [package model] section of the IBIS description.

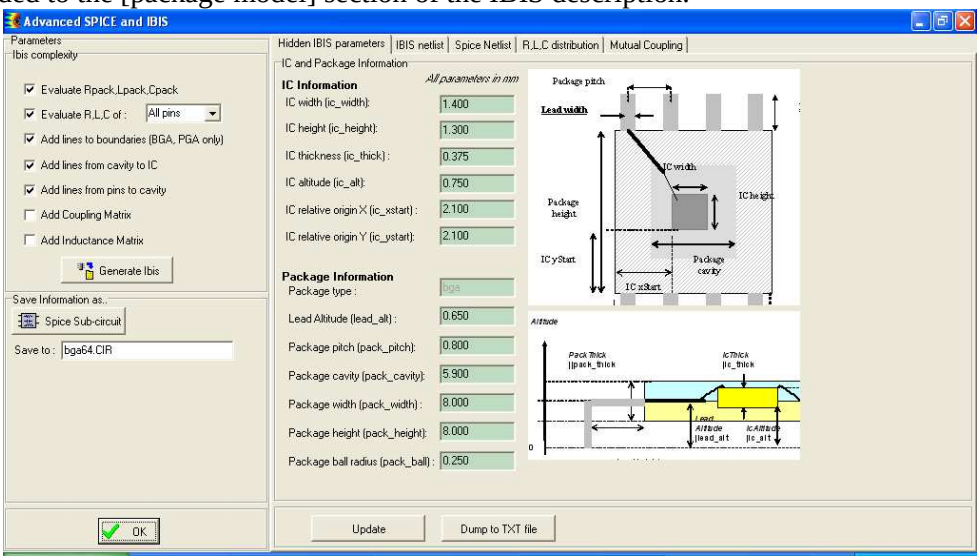


Figure 4-15 : Module "Advanced SPICE and IBIS" on a BGA (Case study/Bga 64/ BGA64.ibs)

The list of hidden parameters is described in section 4.3.1 of this manual. The most important

parameters appear in the main menu of the module, as can be seen in Fig. 4-15. Recall that the hidden keyword information is placed in the [Package model] section, and starts by « | » to avoid parsing errors with conventional IBIS loaders.

4.4.2 How R,L,C are computed

The tool first develops a 2D-geometric floorplan of the leads by calculating the length and position angle of the traces. The 2D view can be observed using the command "EMC → Ibis Interface" (Fig. 4-16).

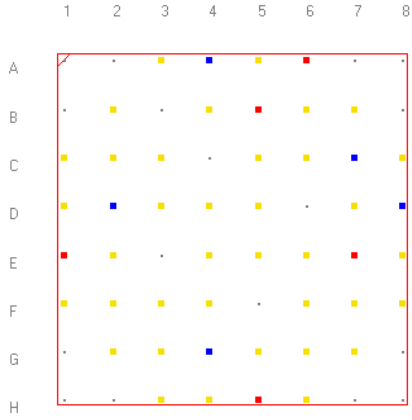


Figure 4-16 : 2D floorplan of a BGA 64 package (Case study/Bga 64/ BGA64.ibs)

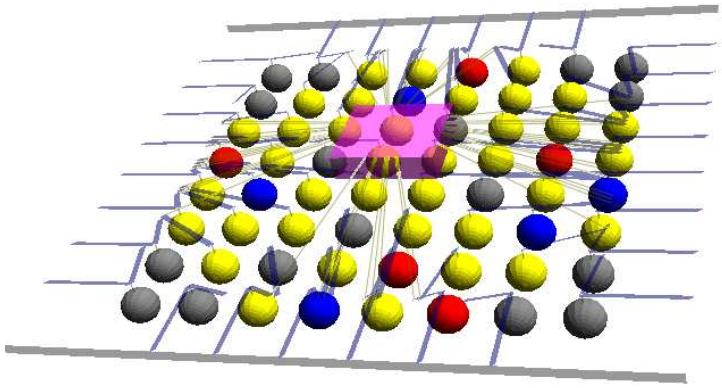


Figure 4-17 : 3D reconstruction of the BGA 64 (Case study/Bga 64/ BGA64.ibs)

Then, the program determines the trace structure, length and position in 3D. Fig. 4-17 shows the 3D reconstruction of the package. The view can be obtained from "Tools → 3D Package Viewer". To obtain reasonably accurate values for R,L and C, analytical formulations as described in section 3.3 – Conductor and Passive Models are employed. Each electrical parts of each wire (bonding, lead, soldier ball) is considered separately. For each elementary electrical wire, we compute:

- the resistance
- the self inductance;
- the capacitance to a ground plane

and optionally:

- the mutual inductance Lx with its nearest neighbors
- the mutual capacitance Cx with its next neighbor

In the BGA, each wire consists of 5 conductor parts, as illustrated in figure 4-18:

1. Ball
2. Ball to Via
3. Via
4. Via to Cavity
5. Cavity to boundaries
6. Cavity to IC

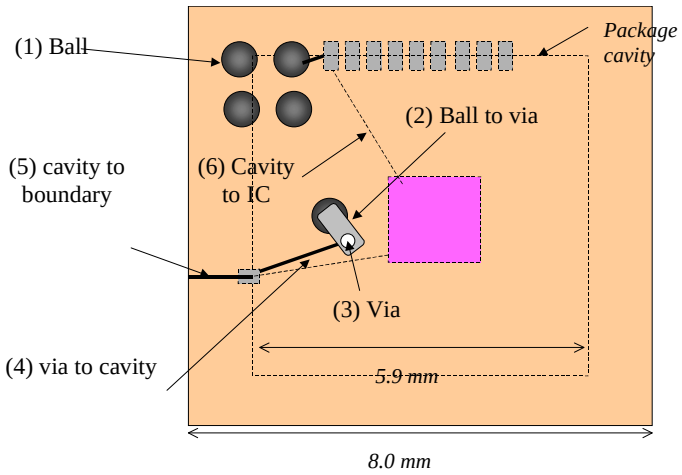


Figure 4-18 : The 6 electrical elements forming each pin of the BGA package

4.4.3 Parasitic R,L,C in Ibis

In IBIS specification, the R,L,C values defined in the [Package] field, items R_pack, L_pkg, C_pkg are provided in a min/typ/max. The tool "Advanced SPICE and IBIS" can determine the parasitic elements of the package in an IBIS compatible format as described in fig. 4-19.

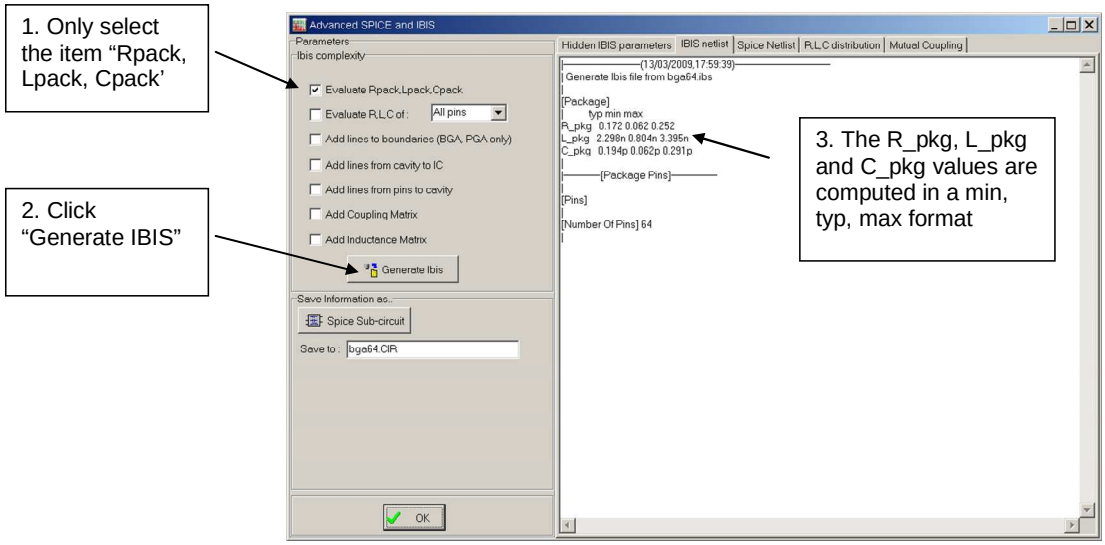


Figure 4-19 : Computing R_pkg, L_pkg and C_pkg in min,typ,max format (Case study/Bga 64/BGA64.ibs)

4.4.4 Complete Ibis Netlist

Select the desired items in the “Ibis complexity” left menu, click “Generate IBIS”, and see the corresponding text in IBIS v4.2 format listed in the right menu “IBIS Netlist”. The text can be copy/paste. In the example shown in Fig. 4-20, the R,L,C parasitic information is added to each pin of the package in the [Pins] section. The values have been deduced from the 3D package reconstruction. The text can be used to update the IBIS file.

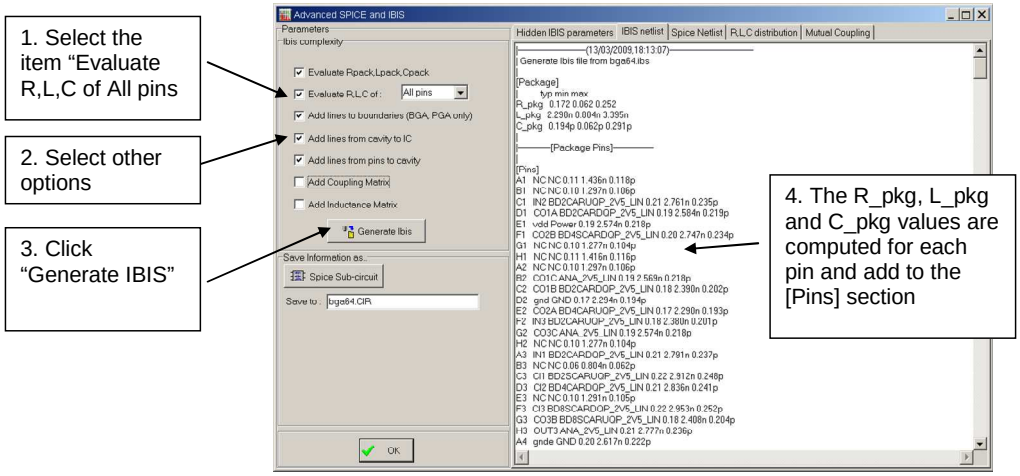


Figure 4-20 : Add R_pkg, L_pkg and C_pkg information for each pin (Case study/Bga 64/BGA64.ibs)

4.4.5 SPICE Netlist

The SPICE netlist contains the same information as for the IBIS netlist, but in a SPICE-compatible format [4-5]. The syntax used to describe the netlist corresponds to a Sub-circuit (keyword SUBCKT). Note that all elements selected in the left menu “Ibis complexity” are described in SPICE format (Fig. 4-21). The subcircuit can be used as it in a larger SPICE simulation.

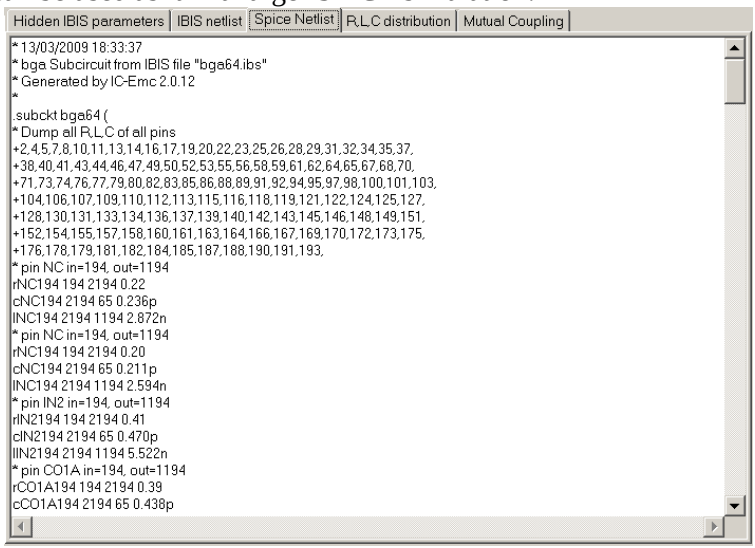


Figure 4-21 : SPICE sub-circuit corresponding to the electric description of R,L and C (Case study/Bga 64/BGA64.ibs)

4.4.6 R,L,C Distribution

The item « R,L,C » distribution is convenient to have a complete view of the inductance, capacitance and resistance values depending on the pin number. In Fig. 4-22, the variation of inductance is bounded by values around 1.2 nH for shortest wires (except one unconnected pin around 0.7nH) and

3.4 nH for the longest wires.

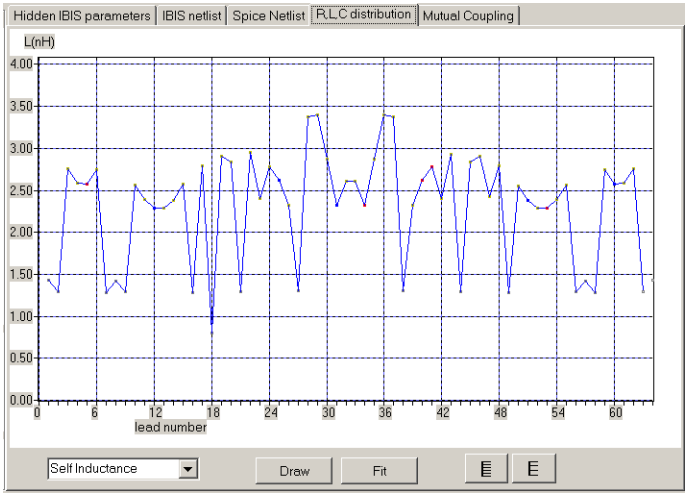
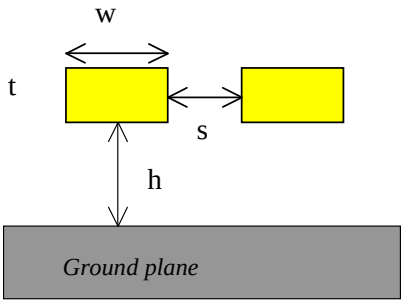


Figure 4-22: Inductance variation versus lead number (Case study/Bga 64/BGA64.ibs)

4.4.7 Mutual Inductance

The program calculates the mutual inductance between the Nth trace and the N-1 trace by using the equation 4-1.



$$L_{12} = \frac{\mu_0}{2\pi}.\ln(\frac{(s+2r)^2+(r+2H)^2}{(s+2r)^2+r^2} \quad \textit{Equ. 4-1}$$

$$r = \frac{t+w}{4}$$

where:
M=mutual inductance per unit length (H/m)
s=separation between conductors (m)
h=height over the ground plane (m)
t=conductor thickness (m)
w=conductor width (m)

The IC-EMC tool stores this data in arrays to be used later when determining the coupling coefficients compatible with SPICE syntax. Mutual inductance is described in SPICE format using K elements as follows.

MUTUAL KXXXXX LYYYY LZZZZ VALUE Example: K1 L1 L2 0.6	LYYYY and LZZZZ are the inductance element names to be coupled. VALUE is the coefficient of coupling between 0 and 1.

$$K = \frac{M}{\sqrt{\frac{L1}{L2}}} \qquad \text{Equ. 4-2}$$

where:
L1 is the inductance of the trace 1 (H)
L2 in the inductance of the trace 2 (H)
M is the mutual inductance between traces 1 and 2 (H)

4.4.8 Inductance Matrix in IBIS

In IBIS version 4.0 and above, the [Inductance Matrix] keyword enables to describe the mutual inductance coupling. Different format can be used for the [Inductance Matrix] data. The most concise format (Sparse_matrix) is used in IC-EMC.
The coefficients for Lij are defined as the voltage induced on conductor "j" when conductor "i'"s current is changed by 1 amp/sec and all other conductors have no current change. The [Inductance Matrix] has symmetry, as the entries below the main diagonal of the matrix are identical to the corresponding entries above the main diagonal. Therefore, only roughly one-half of the matrix needs to be described. By convention, the main diagonal and the UPPER half of the matrix are provided.

The notation [I, J] refers to the entry in row I and column J of the matrix. Note that I and J are allowed to be alphanumeric strings as well as integers. An ordering of these strings is defined in the [Pin Numbers] section.
The numeric entries of the matrices are standard IBIS floating point numbers. As such, it is permissible to use metric "suffix" notation. Thus, an entry of the L matrix could be given as 1.23e-9 or as 1.23n or 1.23nH.
In IBIS version 4.2 [Ref Ibisv4.2], a Sparse_matrix is expected to consist mostly of zero-valued entries, except for a few non zeros. This feature is useful for PGA and BGA package coupling description. An N x N Sparse_matrix is specified one row at a time, starting with row 1 and continuing down to row N. Each new row is marked with the [Row] keyword. For the entry [I, J] of a row, it is necessary to explicitly list the name of pin J before the value of the entry is given. This specification serves to indicate to the parser where the entry is put into the matrix.
Each (Index, Value) pair is listed upon a separate line. Consider the following example. Suppose that row 10 has nonzero entries [10,10], [10,11], [10,15], and [10,25]. The following row data would be provided:

```
[Row]   10
| Index       Value
10          5.7e-9
11          1.1e-9
15          1.1e-9
25          1.1e-9
```

Note that each of the column indices listed for any row must be greater than or equal to the row index, because they always come from the upper half of the matrix. As alphanumeric pin names are used in BGA and PGA, special care must be taken to ensure that the ordering defined in the [Pin Numbers] section is observed.
The list of inductance couplings (noted “Lx”) can be generated using the item “Mutual Coupling” and selecting the button “L Coupling” (Fig. 4-23).

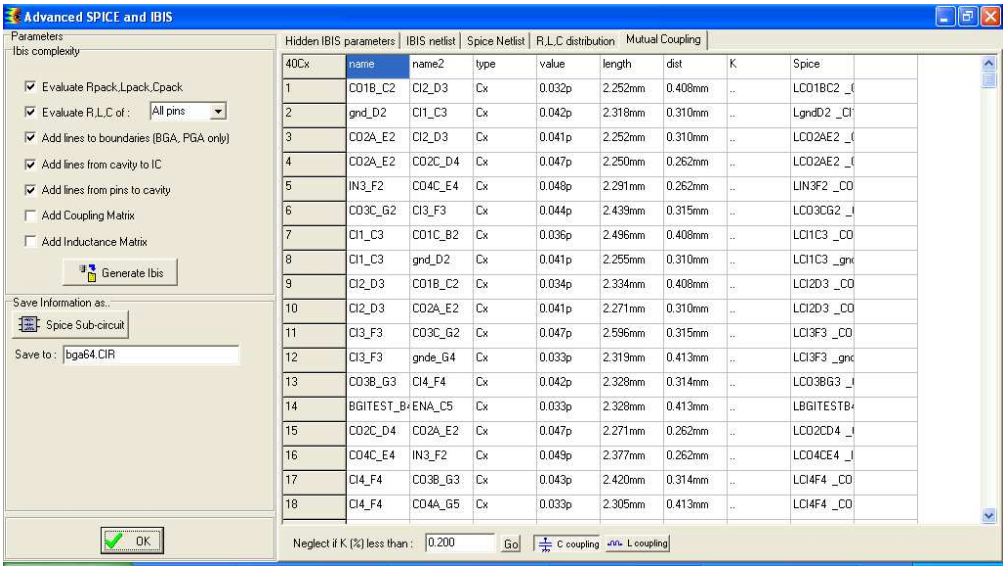


Figure 4-23: Inductance coupling listed in IC-EMC (Case study/Bga 64/BGA64.ibs)

4.4.9 Capacitance matrix in Ibis

The program computes the mutual capacitance of a conductor to all the other conductors that will contribute to its total capacitance. The total capacitance is the sum of the ground capacitance and all mutual capacitors calculated for that ball position except the two nearest neighbors on each side. The list of mutual couplings can be seen in Fig. 4-24.

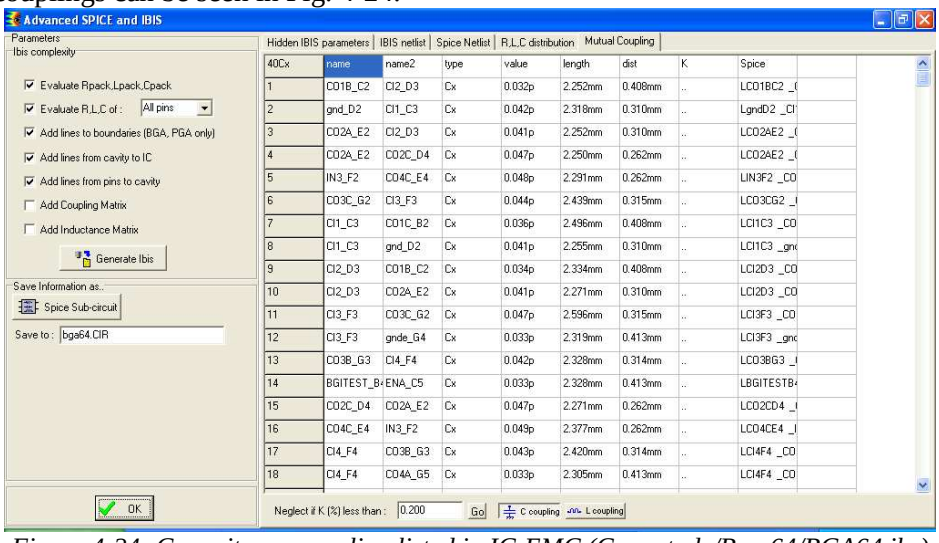


Figure 4-24: Capacitance coupling listed in IC-EMC (Case study/Bga 64/BGA64.ibs)

Values for the package material's dielectric constant and the thickness of the package are defined as hidden keywords in IBIS. The tool also calculates the capacitance to the ground plane. This is performed by using the conductor's length (I), width (w) and thickness (t), the effective dielectric constant of the package and the distance from the conductor to ground plane (H). The Delorme formulations are applied with theses data for all conductors.

A value for total capacitance is given to each conductor of the package which is the sum of all the conductor capacitance to the ground plane for each of the 5 elements. The Cij values are the coupling capacitance between adjacent leads. In IBIS, we use [Capacitance Matrix] for this description.

4.4.10 Resistance matrix in Ibis

Frequency dependent models of resistance can not be inserted in IBIS (cf. section 3.3.1.2). Consequently, the R matrix is computed at a user's defined frequency. It is recommended to fix that frequency to 100 MHz up to 10 GHz depending on the target simulation, as the resistance values are significantly higher that the DC values at such high frequencies

4.4.11 R,L,C matrix insertion in IBIS

The Keyword [Pin Numbers] not only indicates to the parser the set of names that are used for the package pins but also lists the R,L,C elements for each section of a pin's die to pin connection. Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as the number of pins given by the preceding [Number Of Pins] keyword. Each pin name is followed by a combination of *Len, R, L* and *C* sub-parameters (Table 4-4).

Len	The length of a package stub section. Lengths are given in terms of arbitrary 'units'.
L	Inductance of each section, in henries/unit length. For example, if the total inductance of a section is 3.0nH and the length of the section is 2 'units', the inductance would be listed as L = 1.5nH (i.e. 3.0 / 2).
R	The DC (ohmic) resistance of a package stub section, in terms of ohms/unit length.
C	The capacitance of a package stub section, in terms of farads/unit length.

Table 4-4 : Keywords used to insert RLC matrix in IBIS file

A section description begins with the Len sub-parameter and ends with the slash (/) character. The value of the *Len, L, R,* and *C* sub-parameters and the sub-parameter itself are separated by an equals sign (=).

If the *Len* sub-parameter is given as zero, then the L/R/C sub-parameters represent lumped elements. If the *Len* sub-parameter is non-zero, then the L/R/C sub-parameters represent distributed elements.
A three-section package stub description that includes a bond wire (lumped inductance), a trace (treated as a transmission line with DC resistance), and a pin modeled as a lumped L/C element is shown below:

```
|
[Pin Numbers]
A1 Len=0 L=1.2n/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/
|
```

The [Inductance Matrix] and [Capacitance Matrix] are declared in the [Model Data] section that ends with [End Model Data]. The data is a set of three matrices: the resistance (R), inductance (L), and capacitance(C) matrices. Each matrix can be formatted differently.

4.5 Summary

This chapter described the IBIS file through the IBIS interface proposed by IC-EMC. The IBIS interface proposed an editor of IBIS file and different screen to display data included in the file. IBIS is very interesting from an EMC point of view because it can provide valuable information to simulate signal integrity. However, IBIS information alone does not allow simulation of power integrity because IBIS does not take into account of I/O power supply.
IBIS is an open format so that new keywords can be added. In this chapter, several keywords have been added to original IBIS file to provide information about package geometry. These data and the pin list are used by IC-EMC to build a simplified 3D model of the package and extract electrical

models for package pins. This simple method is very helpful to extract package model rapidly and without long electromagnetic simulation.

4.6 References

[4-1] IBIS v2.1: IEC 62014-1: Electronic behavioral specifications of digital integrated circuits I/O Buffer Information Specification, http://www.eigroup.org/ibis

[4-2] R. Leventhal, L. Green, "Semiconductor Modeling for Simulating Signal, Power and Electromagnetic Integrity", Springer, 2006, ISBN 0-387-24159-0

[4-3] B. Ross, "IBIS and ICEM interaction", Microelectronics Journals – Special Issues – 3rd International Workshop on Electromagnetic Compatibility of Integrated Circuits, Vol. 35, No 6, June 2004, pp. 497 – 500, ISSN 0026-2692

[4-4] W. Liu, "MOSFET Models for SPICE simulation including BSIM3V3 and BSIM4", Wiley, 2001, ISBN 0-471-39697-4

[4-5] The SPICE simulator WinSPICE is available at www.winspice.com

4.7 Exercises

1. Exercise 1: I(V) models

Load the IBIS file "ibis\exercise\IBIS_case_study.ibs". It corresponds to the IBIS file of a digital circuit mounted in a QFP64 package. From the I(V) curve, propose a SPICE model for the input and output buffers. SPICE models for diode and transistors of this specific circuit technology are included in a separate SPICE library file "ibis\exercise\spice_case_study.lib".

2. Exercise 2: Signal integrity

The previous output buffer is connected to a 47 pF load through a 3-cm long and 0.508-mm wide PCB track. The track is designed on a 1.6 mm thick FR4 board.

1. From the IBIS file "ibis\exercise\IBIS_case_study.ibs", propose a model for the package.

2. Build the complete model containing the output buffer, the PCB track and the load. Simulate the transient voltage profiles at the buffer output and across the capacitive load. What do you observe? How can you explain the simulation result (it's better to do exercise 3.8 before doing this exercise)?

3. Propose a solution to solve signal integrity issues.

3. Exercise 3 – Simultaneous switching noise

Output buffers are one of the main contributors of parasitic emission of ICs. In this exercise, the simulator IC-EMC is used to investigate the influence of several IC parameters on the conducted noise on power supply lines. We consider a single output buffer, modeled as a CMOS inverter with the given dimensions. Models of MOS transistors are included in the file "ibis\exercise\spice_case_study.lib".
The buffer is driven by a pre-driver stage modeled by a square generator with the following characteristics:

- V0 = 0 V, V1 = 5 V

- Tr = Tf = 1 ns
- Period = 100 ns
- PW = Period – Tr (to keep a 50 % duty cycle)

The output buffer is loaded by a CMOS circuit input buffer, modeled by an equivalent capacitance. The conducted noise flowing on power supply lines is probed across a 1 Ω resistor placed between the ground and the Vss terminal of the buffer.

1. Build the schematic with a 10 pF load. Observe the transient response across the 1 Ω probe. Comment. Deduce the amplitude of dynamic consumption of current.

2. Load the output of the buffer with different values of capacitance (from 10 fF to 1 nF). Observe the transient response of voltage across the 1 Ω probe and comment.

3. Put a 47 pF load at the output of the buffer. Plot the FFT of the noise on Vss. Over which frequency range is located the noise?

4. Do the simulation of question 3 for Tr = 5 ns. What do you observe on the transient response and the FFT of the voltage across the 1 Ω probe?

5. Add a 5-cm long, 0.508-mm wide PCB track designed on a 1.6 mm thick FR4 substrate. Observe the transient response and the spectrum of noise on Vss. Analyze the results.

6. Up to now, the power supply and the reference ground of the buffer have been supposed ideal. However, the package effect has been neglected. The package inductance is evaluated to 10 nH. Does it influences the signal integrity, and/or the power integrity?
Suggestion: plot the transient response on Vdd or Vss.

7. Propose a circuit design solution to attenuate the switching noise on power supplies.

8. The simulated I/O is part of an 8-I/O port, supplied by the same power network. Simulate the noise conducted on the ground reference when all the I/O switch. Find the worst case condition for the noise.

5 Emission Simulation

As integrated circuits are major sources of electromagnetic emission, the primary objective of EMC models of ICs is to feed subsystem-level EMC simulations with simple and accurate models of embedded IC. One of the main features of IC-EMC is the simulation of conducted and radiated electromagnetic emission of circuits. This chapter describes the simulation flow for emission. Note that near-field emission is treated in a separate chapter (chapter 6). Emission models of IC are proposed for a variety of examples, putting the emphasis on standard emission measurement methods at IC level, defined by the standard IEC 61967 [5-1].
Predicting the electromagnetic emission of a circuit is an arduous task, which depends on various and complex parameters (activity of the IC, IC power supply network, PCB routing, external loads…). Modeling accurately the emission of a circuit requires a large set of parameters which are most of the time confidential. Different EMC expert workgroups have developed macro-models to overcome these issues and developed IC models dedicated to emission prediction, as ICEM [5-2] and IMIC [5-3]. The good balance between efficiency and accuracy given by ICEM model has convinced the authors of this software to promote ICEM model, which is introduced in the following pages. IC-EMC also proposes a unique tool dedicated to the automatic generation of ICEM model from a reduced set of IC parameters.

5.1 Characterization of the electromagnetic emission of integrated circuits

In order to ensure the low electromagnetic emission of ICs, they must pass emission test measurements. The characterization of the emission of an IC consists in measuring the conducted or radiated electromagnetic level produced by its activity. The test should isolate as much as possible the effect of the circuit on electromagnetic emission, even if it is also influenced by parameters external to the circuit (decoupling capacitor placement, board routing, I/O loads). The standard IEC 61967 defines methods to characterize IC emission over the frequency range 150 KHz – 1 GHz [5-1]. Table 5-1 and 5-2 sums up the standard methods for characterization of IC emission according to IEC 61967 and their status.

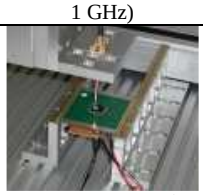
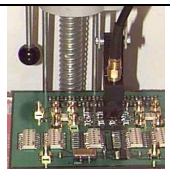
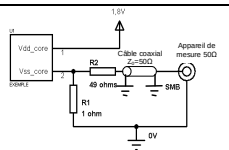
 IEC 61967-2 (TEM cell : 1 GHz)	 IEC 61967-2 (GTEM cell : 18 GHz)	 IEC 61967-5 (WBFC: 1 GHz)	 IEC 61967-8 (IC stripline: 3 / 6 GHz)
 IEC 61967-3 (Near field scan : 1/ 5 GHz)	 IEC 61967-6 (magnetic probe: 1 GHz)	 IEC 61967-4 (1/150 ohm : 1 GHz)	 IEC 61967-7 (Mode stirred chamber : 1 GHz)

Table 5-1 : Measurement methods related to the IC emission standards IEC 61967 [5-1]

5.2 Flow for Emission Simulation

Most of the time, EMC of IC models are validated by measurements done on a circuit mounted on specific EMC board, in a minimalist configuration. Once the circuit model has been tuned with measurements and validated, it can be included in a subsystem model to simulate the emission of a complete electronic systems, which may include several circuits, PCB tracks and planes, connectors, cables…. One key objective of IC-EMC is to help the user to build EMC models and ease the comparison with EMC measurements.

Standard	Description	Stage in 2011
IEC 61967-1	General conditions and definitions	Standard
IEC 61967-2	TEM cell and wideband TEM (GTEM) cell method	Standard
IEC 61967-3	Surface scan method	Standard
IEC 61967-4	1 Ω/150 Ω direct coupling method	Standard
IEC 61967-5	Workbench Faraday Cage method (WBFC)	Standard
IEC 61967-6	Magnetic probe method	Standard
IEC 61967-7	Mode Stirred Chamber method (CRBM)	Proposal
IEC 61967-8	IC Stripline method	Proposal

Table 5-2 : Status in 2011 of standard IEC 61967 - Measurement of IC susceptibility up to 1GHz [5-1]

The general flow used to compare measurement and simulation is described in figure 5-1. It takes the example of a conducted emission measurement based on the standard IEC 61967-4 – 1 Ω/150 Ω [5-4]. This method is based on the use of measurement probes (1 Ω or 150 Ω) designed on the test board and placed on EMC-sensitive pins such as power supply, ground or digital output pins.

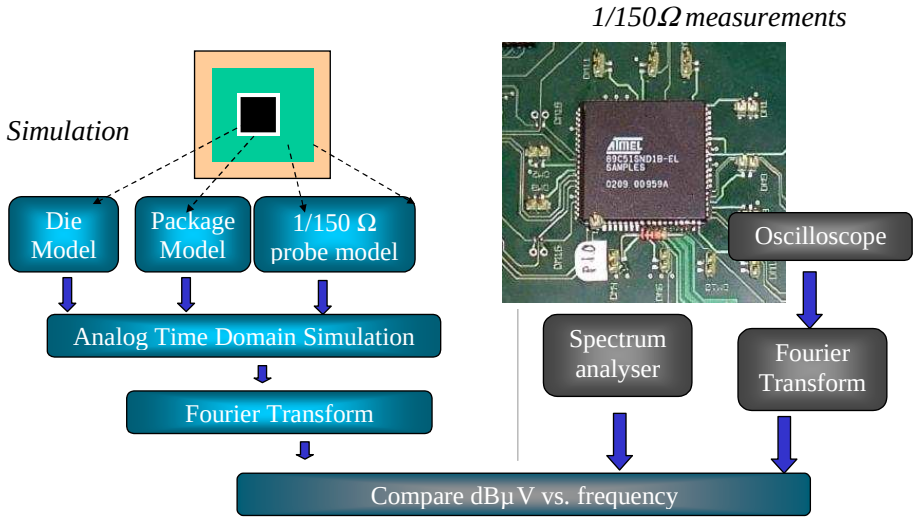


Figure 5-1 : 1/150Ω simulation vs. measurements

Emission measurements are traditionally performed in frequency domain. Measurements may also be done using wideband oscilloscopes and active probes, which can be converted into frequency domain using a Fourier Transform.

As electromagnetic emission originates from transient activity of circuits, simulations in IC-EMC are performed in time domain. Spectrums of electromagnetic interferences produced by circuits are then extracted with a FFT algorithm.

The simulation steps for comparing measured and simulated electromagnetic emission under IC-EMC are described in figure 5-2. Ideally, models are built from IBIS and ICEM model provided by the IC supplier. The ibis file contains I/O and package information. Using WinSpice, the circuit is simulated in time-domain to get its current and voltage variations. The tool IC-EMC enables the exploitation of these simulations in order to compare the results with conducted mode and radiated mode measurements according to international standard methods described in [5-1].

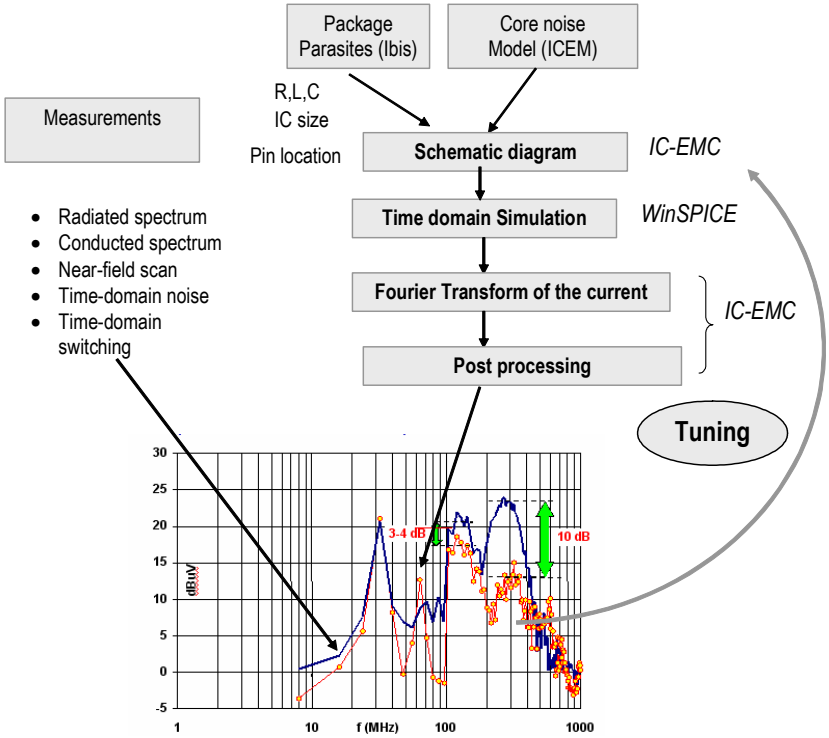


Figure 5-2: Exploitation of ICEM and IBIS models to compare simulation and measurements

5.3 The ICEM model

The main objective of the ICEM model (Integrated Circuit Emission Model) for components is to propose electrical modeling for analog or digital integrated circuit internal activities up to 3 GHz. The ICEM proposal was issued in 2002 by the UTE task force (see above the associated logo). The technical report has been standardized by the IEC committee under reference IEC 62014-3 in 2004 [5-5]. In 2006, ICEM and some competing models were included in a general standard called IEC 62433 dedicated to EMC of IC modeling [5-6].
The ICEM approach can be used to:

- Predict conducted and radiated emissions at chip and printed circuit board level
- Predict the auto-compatibility of the circuit (low level immunity analysis)

5.3.1 Definitions

Five types of components have been defined:

- The Internal Activity (IA), which describes the integrated circuit activity by a current source.
- The Passive Decoupling Network (PDN), which describes the impedance network across one or several terminals.
- The Inter-Block Coupling (IBC), which describes the coupling between 2 terminals (for example substrate coupling).
- The External Terminal (ET), which connections with the external environment (IOs,

equivalent dipole for radiated emissions)

- The Internal Terminal (IT), which connections between other on-chip components

In short, an ICEM model of an integrated circuit is composed of a noise source (called Internal Activity or IA), an on-chip passive distribution network (PDN) and a package distribution network, as illustrated in fig. 5-3.

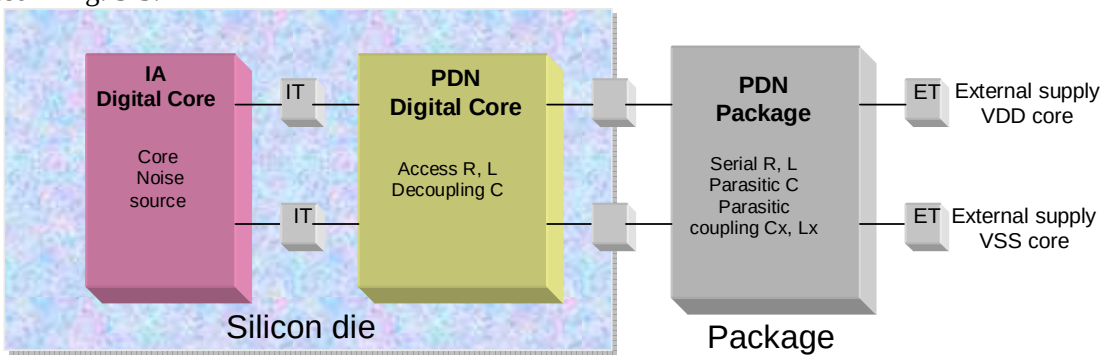


Figure 5-3 : The basic structure of the EMC model of an IC

5.3.2 Getting Started

The passive distribution network describes an impedance structure between terminals. PDN is usually formed by an R,L,C network. There is a distinction between the package PDN, mainly inductive and the on-chip PDN, usually resistive and capacitive. A very simple and generic ICEM model structure is proposed in Fig. 5-4 where the package PDN is simply the power rail inductance (*LPackVdd*, *LpackVss*) and the on-chip PDN is built from R,L,C elements. The simplest Internal Activity (*IA*) model is a current source which represents the current consumption of the die. The *IA* generates violent switching noise inside the logic block, which propagates through the on-chip PDN, then through the package PDN and finally to external printed circuit board (PCB) traces. The external noise is therefore a filtered version of the internal noise. Its amplitude is strongly attenuated by the *PDN*, as compared to the *IA* current pulses.

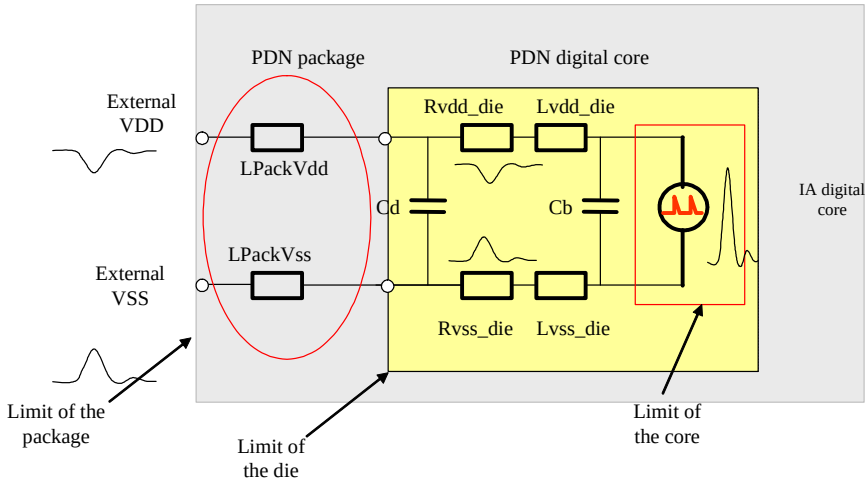


Figure 5-4 : the Internal Activity (IA) and Passive distribution Networks (PDN)

A short description of the ICEM sub-parameters is provided in table 5-3. The complete description may be found in the ICEM cookbook [5-7]. The core model structure includes the global decoupling capacitance *Cd*, the serial resistance *Rvdd_die*, *RVss_die* and serial inductance *Lvdd_die*, *Lvss_die* on the supply rails. The block capacitance *Cb* is close from the current generator *IA* (Figure 5-4).

IA	Current source. Unit: Ampere Description: pulse or piece-wise-linear	Main source of parasitic emission considered in the model is the current source IA. The current shape may consist either of the time-domain description of the current versus time or as an equivalent triangular waveform. Typical values for IA current peak are [100 mA - 100 A] for the amplitude, 0.5 to 5 ns for duration, and 500 ps to 100 ns for the period. More details in the next section.
Cd	Decoupling capacitance. Unit: Farad Description: discrete C	On-chip decoupling capacitance between VDD and VSS. Cd is a physical coupling between the internal supply rails VDD (positive supply) and the ground rail VSS (0V supply). The origin of the capacitance Cd is rail to rail or junction capacitance. Typical value ranges from 100pF (very small Ics) up to 100 nF (very large ICs).
LpackVdd, LpackVss	Equivalent supply inductance of the package. Unit: Henry Description: discrete L	The package inductance Lpack_vdd, Lpack_vss is the equivalent serial inductance of the supply path VDD and VSS. Typical value ranges from 0.1 nH (very short connection to supply, multiple supplies) up to 10 nH (long leads in DIL packages).
Lvdd_die, Lvss_die	Serial internal inductance. Unit: Henry Description: discrete L	The serial inductance Lvdd_die, Lvss_die, in serial with the local block capacitance Cb creates a high frequency resonance effect. Typical value ranges from 0.1 nH (very short connection to supply) up to 10 nH (long connection).
Rvdd_die, Rvss_die	Serial internal resistance. Unit: Ohm Description: discrete R	The serial resistance of the supply network models the path that connects the block supply to the main supply ring. Typical value for Rvdd, Rvss are 0.5 to 50 ohm.
Cb	Block decoupling capacitance. Unit: Farad Description: discrete C	The local block decoupling Cb is the local supply-to-ground capacitance placed in serial with the local current generator Id. It accounts for the equivalent decoupling capacitance of the block. Typical values range from 10 pF to 1 nF.

Table 5-3 : Details on the ICEM discrete components

5.3.3 Internal Activity Model

The Internal Activity model corresponds to one or more current sources. The current generator represents the switching activity of the digital core. The global current peak corresponds to the sum of the current consumption of each elementary block. For example, a CPU comprises between 3000 and 300,000 internal logic gates depending on its complexity (Table 5-4). For each clock cycle, only a weak portion (10%) of these logical gates is active.

CPU generation	Total number of logical gates	Logical active gate during a clock cycle
8 bits	3000-5000	300-500
16 bits	15,000-100,000	1500-10,000
32 bits	50,000-300,000	5000-30,000

Table 5-4 : CPU complexity and gate activity

Table 5-5 details the supply voltage, gate density per mm^2, clock frequency, current per gate and switching speed in typical loading conditions for all major CMOS technology nodes. Considering a 16-bit microcontroller with 10,000 logical gates switching simultaneously, the resulting current peak would be approximately 4,5 A. Currently, gates and interconnects delays spread out the current peak approximately by a factor 10. In order to preserve energy, the amplitude of the peak is divided by 10. A peak of 450 mA on 4 ns is thus obtained as shown in Fig. 5-5.

Technology	Year	Supply	Density of cells /mm^2	Clock frequency (MHz)	Typ. current per gate	Typ. switching delay in typ. loading conditions
0.8µm	1990	5 V	15 K	4-90	0.9 mA	0.5ns
0.5µm	1993	5 V	28 K	8-120	0.7 mA	0.3ns
0.35µm	1995	5-3.3 V	50 K	16-300	0.6 mA	0.2ns
0.25µm	1997	5-2.5 V	90 K	40-450	0.4 mA	0.12ns
0.18µm	1999	3.3-2.0 V	160 K	100-900	0.3 mA	0.1ns
0.12µm	2001	2.5-1.2 V	240 K	150-1200	0.2 mA	70 ps
90 nm	2004	2.5-1.0 V	480 K	300-2000	0.15mA	40 ps
65 nm	2007	2.5-1.0 V	900 K	500-3000	0.1 mA	25 ps
45 nm	2009	2.5-0.7 V	1500 K	800-5000	0.08 mA	15 ps
32 nm	2011	1.8-0.7 V	2500 K	1000-7000	0.06 mA	10 ps
22 nm	2014	1.0-0.6 V	4000 K	1000-10000	0.05 mA	7 ps

Table 5-5 : Typical current per gate and corresponding switching delay for various technologies

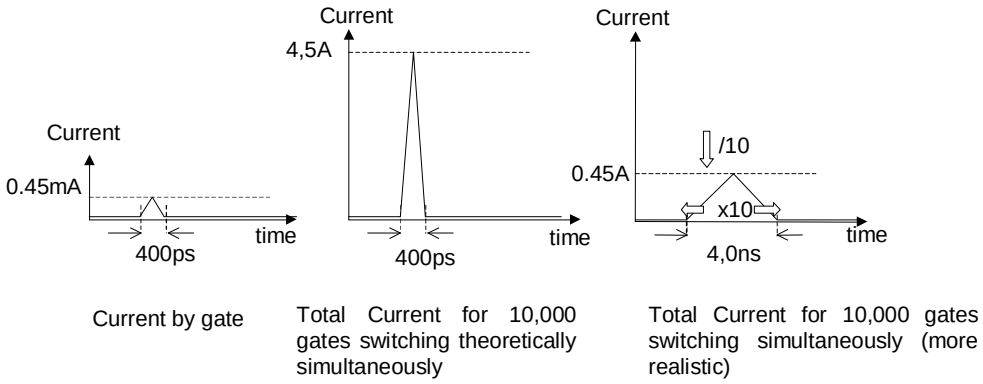


Figure 5-5 : Current peak spread

5.3.4 ICEM at work

The decoupling capacitance *Cd* combined with the package inductance *LpackVdd* and *LpackVss* create a resonant network at the origin of a primary resonance. The serial inductance *Lvdd*, *Lvss*, in serial with the local block capacitance *Cb* creates a high frequency resonance effect. The dominant effect is usually the *Lpack/Cd* resonance (Figure 5-6).

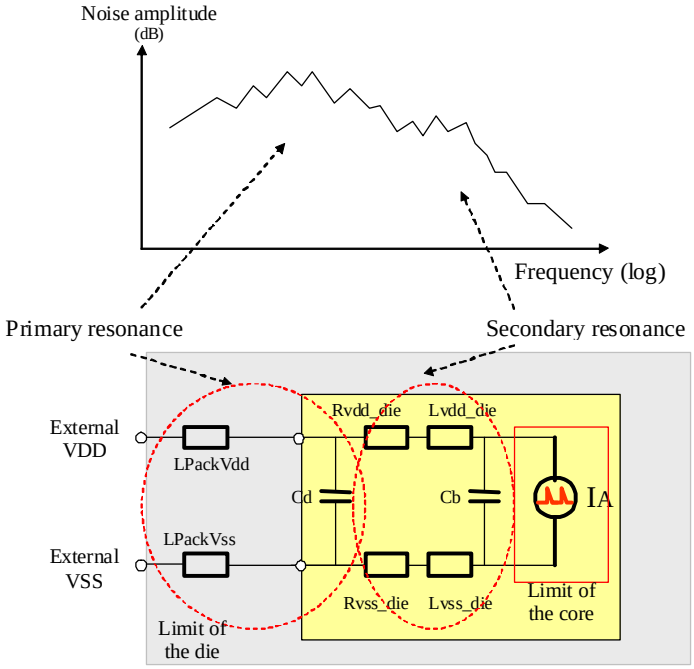


Figure 5-6 : Primary and secondary resonance effects modeled by ICEM

5.3.5 Towards a General Standard Model

In parallel to the ICEM technical report IEC 62014-3, a more ambitious standard for EMC modeling at IC level is under discussion at the IEC working groups under project name IEC 62433. In this document, not only the conducted and radiated emissions are covered, but also the conducted, radiated and impulse immunity. As defined in the draft standard IEC 62433 « Integrated circuits – EMC IC Modelling » [5-6], the following parts are addressed:

- Part 1: General modeling framework
- Part 2: Conducted RF emission. The objective of ICEM-CE (**Integrated Circuit Emission Model**- conducted mode) is to propose a model to describe the conducted emissions of an Integrated circuit. This model is a generalized approach of the ICEM technical report IEC 62014-3.
- Part 3: Radiated RF emission. A draft is under discussion at UTE and IEC levels, based on technical information provided by academic and industrial contributors. The present document is intended to promote both the TEM coupling model (See Appendix E) and the near-field radiated model based on current dipoles.
- Part 4: Conducted RF immunity. Discussions have started at UTE and IEC working groups about this new topic. The present document is intended to promote concepts on conducted RF immunity based on the reuse of ICEM models and accurate modeling of injection devices including the coupler (See section on immunity).
- Part 5: Radiated RF immunity. Original methods based on near-field injection have recently been proposed by the authors, to be promoted to UTE and IEC committees [5-8].
- Part 6: Impulse immunity. Discussions have started at UTE and IEC working groups about this new topic. No work has yet been conduced at INSA about this topic.
- Part 7: Intra-IC modeling. A draft is under discussion at UTE and IEC levels, based on technical information provided by academic and industrial contributors.

Figure 5-7 shows the general structure of the ICEM model which applies for emission analysis. A distinction is made between the digital core, the analog core and the IOs. In the case of mixed signal ICs, a distinction is made between the digital and analog blocks. Supply connections are separate (VDD analog, VDD core, VDD io). Notice the inter-block coupling which models mainly the parasitic substrate coupling between blocks, responsible of a resistive path that couples ground references. From fig. 5-7, it can be seen that a general EMC model is built around a set of ICEM blocks. The structural description of each block is not covered by the standard.

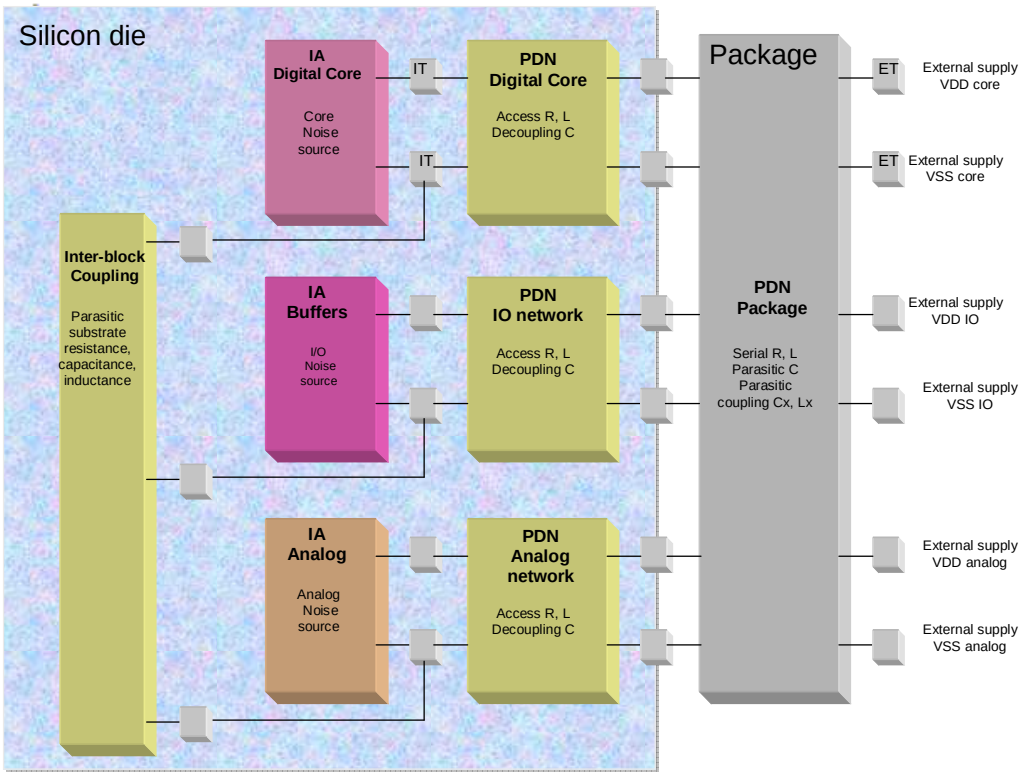


Figure 5-7 : Generic EMC model for ICs proposed in IEC 62433 draft standard

5.4 Case study – Conducted emission of HC12D60

Load the file "d60_vde.sch" which corresponds to figure 5-8. The on-chip PDN of the 16-bit micro-controller is described using basic R,L and C elements. The package PDN is simply a set of inductances with a value extracted from an approximation of the package lead and bonding. The 1 Ω method is modeled by discrete resistances as implemented on the board.

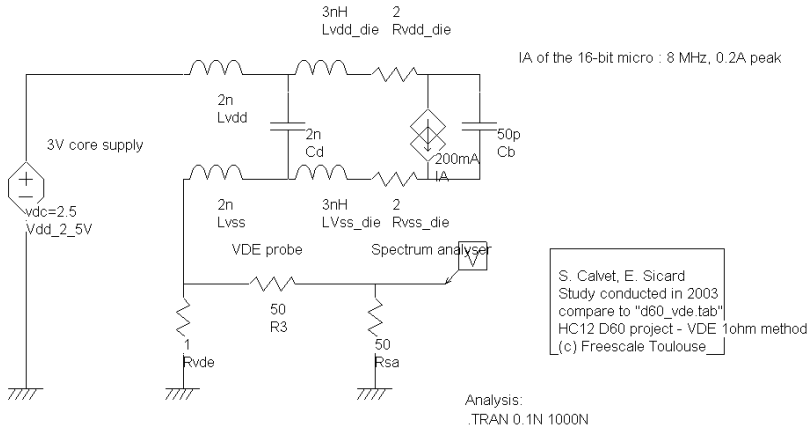


Figure 5-8: The ICEM model of a 16-bit micro-controller (emission/d60/d60_vde.SCH)

Table 5-6 describes the different electrical elements of the ICEM model of the D60 component. Using the tool “Tools → LC Resonant Frequency”, we can compute an LC resonance effect around 410 MHz (Fig. 5-9).

Parameter	Description	Remarks
Ib	Current source. Unit: Ampere Description: piece-wise-linear	The Ib current is described as a periodic triangle (0.2 A max)
Cd	Decoupling capacitance. Unit: Farad Description: discrete C	Cd is 2 nF, which is quite high due to on-chip added capacitance
Lvdd_die, Lvss_die	Serial internal inductance. Unit: Henry Description: discrete L	The serial inductance is tuned to 3 nH, which provokes a resonance effect with Cb around 400 MHz.
Rvdd_die, Rvss_die	Serial internal resistance. Unit: Ohm Description: discrete R	Around 2 ohm serial resistance due to long metal tracks on-chip
Cb	Block decoupling capacitance. Unit: Farad Description: discrete C	Local block capacitance, around 50pF.

Table 5-6 : Description of D60 ICEM elements

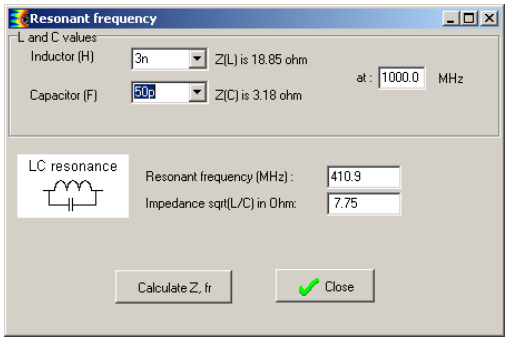


Figure 5-9 : evaluation of the LC resonant frequency

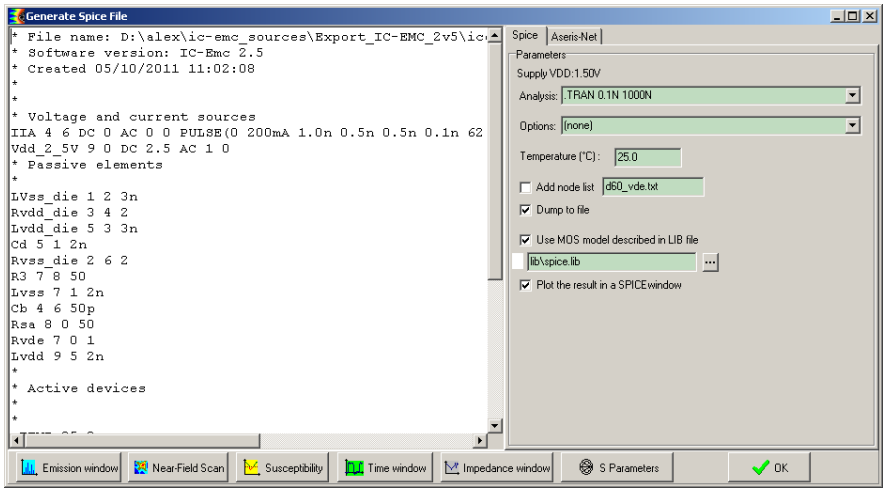


Figure 5-10: SPICE file generated from the schematic diagram (emission/d60/d60_vde.CIR)

Invoke the command *File → Generate Spice file* or click <Ctrl>+<G>. A SPICE-compatible file "d60_vde.CIR" is generated. The following screen appears. Description of the generated SPICE file is given in table 5-7. The description of ICEM parameters in SPICE is based on SPICE reference manual [5-9]. Start the WinSpice program, and click "File" → "Open". Select the desired .CIR file ("d60_vde.CIR"). The simulation is performed in time domain, and the following screen appears (Fig. 5-11). The .TRAN analysis is conducted during 1000 NS. The result is stored in a file called d60_vde.txt.

RESISTOR RXXXXXXX N1 N2 VALUE Example: Rvss 3 7 2ohm	N1 and N2 are the two element nodes. VALUE is the resistance (in ohms) and should be positive.
CAPACITOR CXXXXXXX N+ N- VALUE <IC=INCOND> Example: Cb 6 2 1n	N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance in Farads.
INDUCTOR LYYYYYYY N+ N- VALUE Example: Lvss 8 2 2n	N+ and N- are the positive and negative element nodes, respectively. VALUE is the inductance in Henry.
CURRENT SOURCE IYYYYYYY N+ N- <<DC> DC/TRAN VALUE> Example: IB 23 21 DC 0.01	N+ and N- are the positive and negative nodes, respectively. A current source of positive value forces current to flow out of the N+ node, through the source, and into the N- node. DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is time-invariant (e.g., a power supply), then the value may optionally be preceded by the letters DC.
Supply voltage VYYYYYYY N+ N- <<DC> DC/TRAN VALUE> Example: VDD 1 0 DC 2.0V	N+ and N- are the positive and negative nodes, respectively. A voltage source of positive value is set between N+ node, and N- node.

Table 5-7: List of basic electrical components used in "d60_vde.CIR"

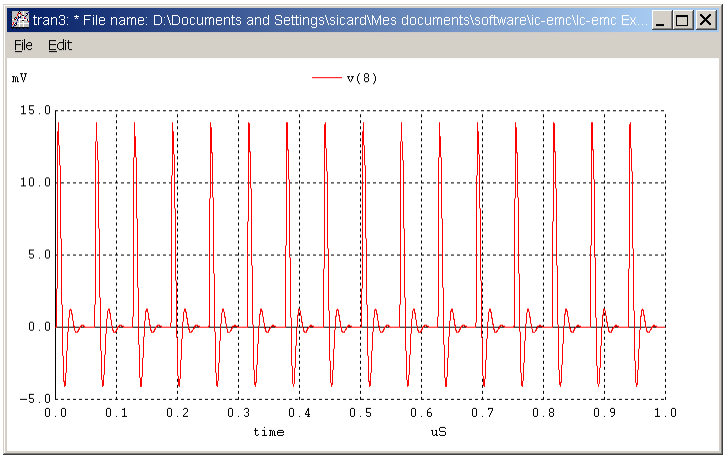


Figure 5-11: the transient simulation performed by WinSpice (emission/d60/d60_vde.cir)

In the SPICE generator menu, click "Emission Window", or click "View" → "Emission dBµV vs. Frequency". The spectrum appears as shown in figure 5-12. It corresponds to the FFT or the WinSpice output file "d60_vde.txt". The FFT points are adapted to fit the information included in the simulation. Click "Add Measurements" and select the measurement file "d60_vde.tab". The measurements are superimposed to the simulations for comparison purpose (Fig. 5-12).
The simulation is well fitted with measurements, as seen in figure 5-12. The main spectrum energy is concentrated in the range 10-300 MHz, with low levels of energy above 500 MHz (above 500 MHz, measured emission reach the noise floor of the spectrum analyzer). The ICEM model remarkably predicts the 50-500 MHz harmonics. However, some discrepancies are observed above 500 MHz.

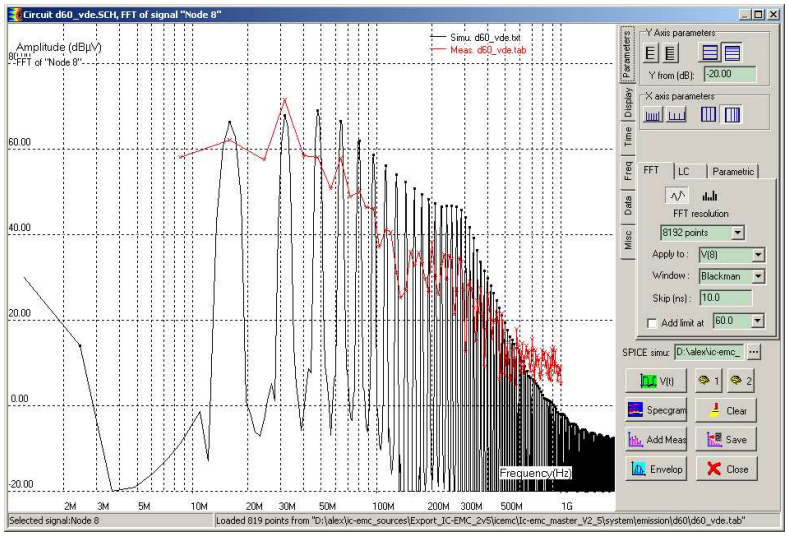


Figure 5-12: Simulation of the conducted emission of the 16-bit microcontroller D60 (d60_vde.sch, d60_vde.tab)

The ICEM parameters may be fitted to improve the accuracy of the prediction in that range. Possible approaches may consist in:

- ⇒ Altering the PULSE current parameters: the rise slope TR or fall slop TF may be modified, as well as the peak current value (I2).
- ⇒ Add a parasitic serial resistance to the decoupling capacitance *Cb*. The value is usual small (some Ω). This will limit the decoupling effect above several hundreds of MHz.
- ⇒ Replacing the PULSE current by a PWL current. The current generator is simply a triangular peak, while the real current is far more complex. The PWL current includes more information which may change the harmonic contents, and thus improve the matching between measurement and simulation.
- ⇒ Alter the values of the block capacitor *Cb* and the serial inductor *Lvdd_die, LVss_die*. This modifies the second order resonance effect.

5.5 Case study – Radiated emission of CESAME Test Chip

The CESAME test chip was dedicated to the characterization of conducted and radiated emissions from six identical logic cores, each having a specific design technique which aims to reduce parasitic emissions. Within the frame of the European project MEDEA+ “MESDIE”, in partnership with ST-Microelectronics and EADS, the main goal of the test chip was to validate these design rules and to quantify the benefits in terms of reduction of parasitic interferences. The most interesting results have been presented in [5-10]. In this section, the use of ICEM for predicting the measured radiated emission in TEM/GTEM cell is described through the case study of CESAME.

5.5.1 Presentation of the component

The internal structure of CESAME is outlined in Fig. 5-13. Six logic core blocks are implemented in the same die. All these blocks have an identical structure based on latches, a clock tree and standard gate which reflect a standard core activity. Among these cores, two structures are worth of interest in our study: the normal core called “NORM” which is supposed to be noisy, and the “RC” core with includes a series resistor on the supply tracks and a local on-chip decoupling to feature low parasitic emission.

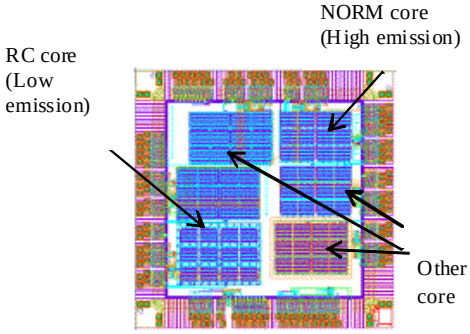


Figure 5-13: The CESAME test chip

An electrical model has been setup for conducted and radiated emission prediction. The current sources that form the Internal Activity (IA) are identical for NORM and RC core. The main difference concerns the serial resistance (*Rdd_die, Rvss-die*) and the local decoupling capacitance *Cb*. The access inductance of the package is almost the same for RC and NORM cores.

Load the file "cesame_norm_vde.sch" which corresponds to figure 5-14. The on-chip PDN of this test-chip is described using basic R,L,C elements. The package PDN is again reduced to two inductances. Compared to the D60 case study, the only differences lie in the serial resistance *Rcd* and *Rcb* with the decoupling capacitance. These resistances account for the non-perfect conductor path to the distributed decoupling. The comparison between measured and simulated emission for the CESAME core test-chip is given in fig. 5-15. The measurement file is “cesame_vde_norm.tab”.

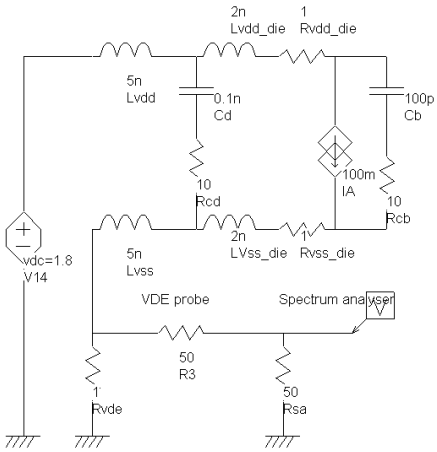


Figure 5-14 : CESAME case study (emission/cesame/cesame_vde_norm.SCH)

The fitting is good on the 200-600 MHz harmonics, while the model overestimates the 100 MHz peak. The IA clock is a perfect triangle while the real-case IC is more a two-phase system. Note the 1.8 GHz harmonic in the measurement which corresponds to the EMI interference with DCS mobile phone band, and not to any radiated emission form the IC itself.

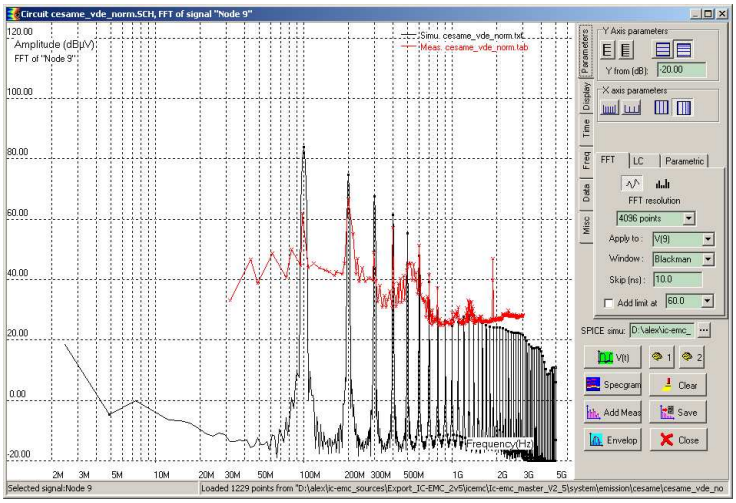


Figure 5-15 : Comparing measured and conducted emission in the CESAME NORM test chip (cesame_vde_norm.sch, cesame_vde_norm.tab)

5.5.2 The TEM Cell Method

The flow to compare TEM measurement (IEC 61967-2) [5-11] and simulation is given in figure 5-16. The approach used for the circuit modeling is based on ICEM. We must consider the die, package, TEM cell and coupling models. Once the model is completed, an analog time domain simulation is performed. For comparison purpose, the time-domain waveform is translated into frequency domain and plotted in log/log scale for comparison with the measurements obtained by the spectrum analyzer.

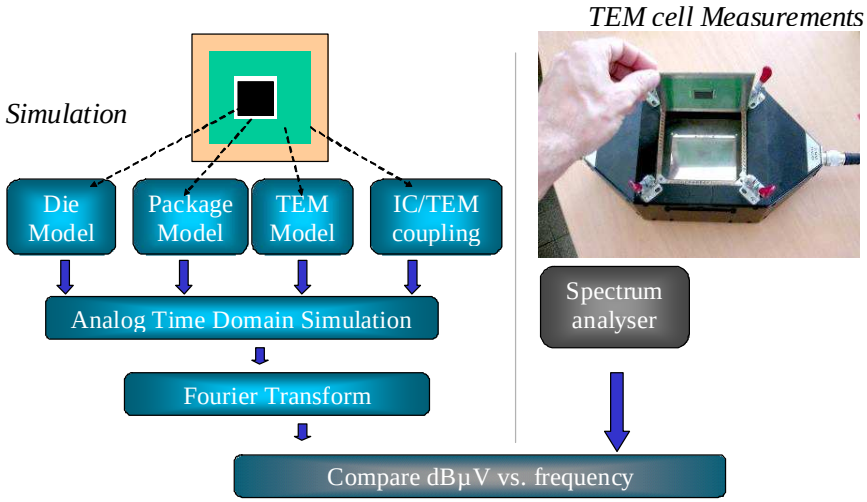


Figure 5-16 : TEM Cell simulation vs. measurements

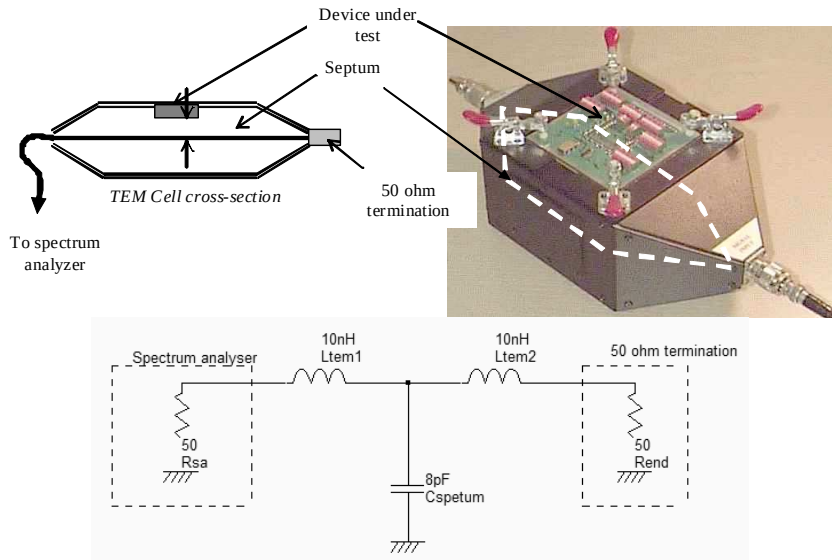


Figure 5-17 : The TEM cell model (emission/temcell/temModel.SCH)

Note that the same die and package models may be used for conducted and radiated emission predictions. The TEM cell picture and model are proposed in figure 5-17. The core of the cell consists in a 50-Ω adapted metal plate in a grounded chamber. The metal plate is called septum. The simple septum model consists of two inductors and a capacitor. For symmetry, the total septum inductor is split into two inductors *Ltem1* and *Ltem2*, 10 nH each. The capacitance of the septum vs. the ground is around 8pF. This model is valid until 1 GHz.

5.5.3 Coupling between the IC and the TEM Cell

For TEM cell modeling, two main coupling phenomena have been identified:

- Capacitance coupling between the die and the septum

- Inductance coupling between the package and the septum

The mutual inductance coupling can be evaluated with the following formula:

$$k = \frac{L_{12}}{\sqrt{L_1 \times L_2}} \qquad \textit{Equ. 5-1}$$

Where:
K = coupling coefficient (0 to 1, 1= maximum coupling)
L12 = mutual inductance (H)
L1 = inductance value 1 (H)
L2 = inductance value 2 (H)

The capacitance coupling between the IC and the septum is represented by *Cx*, with a value of 100 fF (Figure 5-18). The inductance coupling between the VDD supply inductance *Lvdd* and the septum inductance *Ltem1*, *Ltem2* is represented by a coupling factor K as defined in equation 5-1.

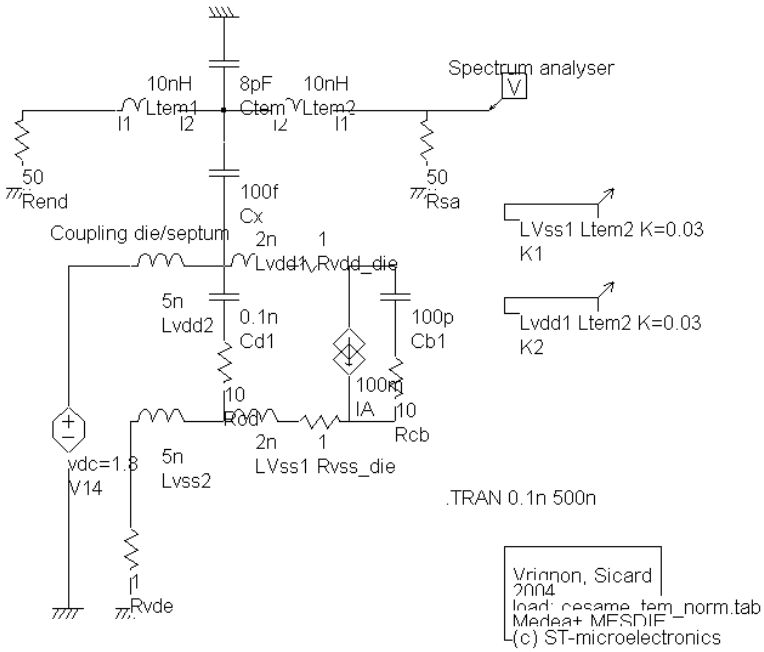


Figure 5-18 : A model of the CESAME test chip in the TEM cell (emission/cesame/cesame_tem_norm.sch)

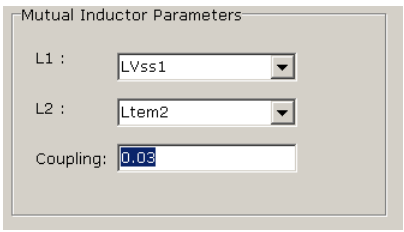


Figure 5-19: Modifying the coupling factor between two inductors

```
Kxxx Lyyy Lzzz coef
Example: K1 Ltem2 Lvdd1 0.03
```

The coupling element K is added either as a label with following syntax or by a specific component called “Mutual Coupling” that may be found in the symbol palette. To modify the coupling value, double click inside the symbol (or in the label), and change the number associated to the field “Coupling” (Fig. 5-19) to the desired value.

5.5.4 Comparison between TEM measurements and simulations

A comparison between measurements (In red) and simulation (In black) is proposed in figure 5-20. It can be seen that a reasonable agreement is found up to 1 GHz. The simulation is a little lower than measurements around 200 MHz. Notice that the I/O switching that occurs in real-case measurements at a rate of 10 MHz provokes harmonics starting from 10 MHz. In the model, this switching has been ignored. Adding these switchings would probably add sub-harmonics and rise the level of 100-300 MHz harmonics as well, for a better matching with measurements.
Worth of interest is the fact that the same model has been used both for conducted emission prediction and for TEM cell radiated emission. The reuse of the same ICEM model for as many setups as possible is one of the key goals of these EMC studies.

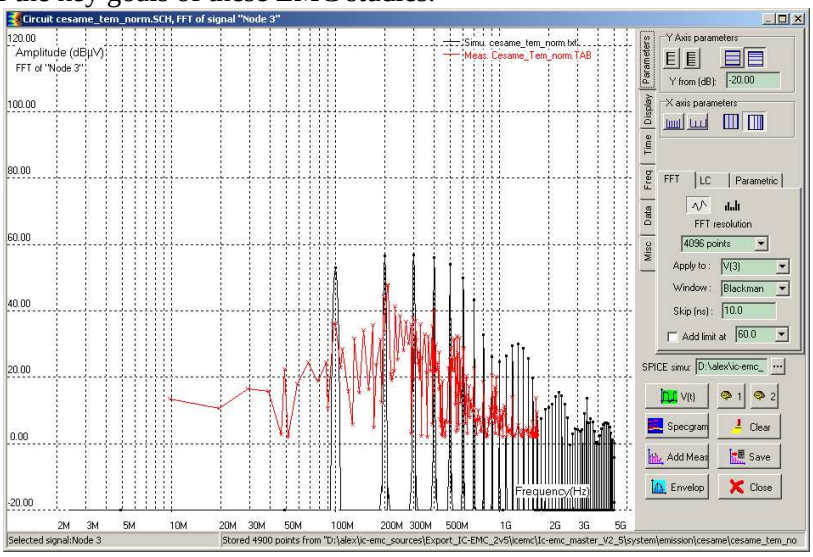


Figure 5-20 : Comparing simulation and measurements of the CESAME test chip in the TEM cell (emission/cesame/cesame_tem_norm.sch)

5.6 Predictive analysis using ICEM Models - TriCore Case Study

The purpose of this section is to describe how a simple and non-confidential model can be constructed using the tool **Tools → Icem Model Expert**). This tool aims at generating automatically an ICEM model from high-level specifications of the integrated circuit technology, topology and gate complexity.

5.6.1 Description of the tool

The screen of the ICEM model expert is reported in figure 5-21. On the left upper corner of the window, the default technological parameters are listed. These parameters are provided in the configuration file “default.tec” (CMOS 0.25 µm techgnology), which is described in the appendix. The parameters worth of interest are:

- The typical switching current per gate (0.2 mA in this technology)
- The typical duration of the gate switching (50 ps in the above example)
- The default gate decoupling capacitance (5 fF)

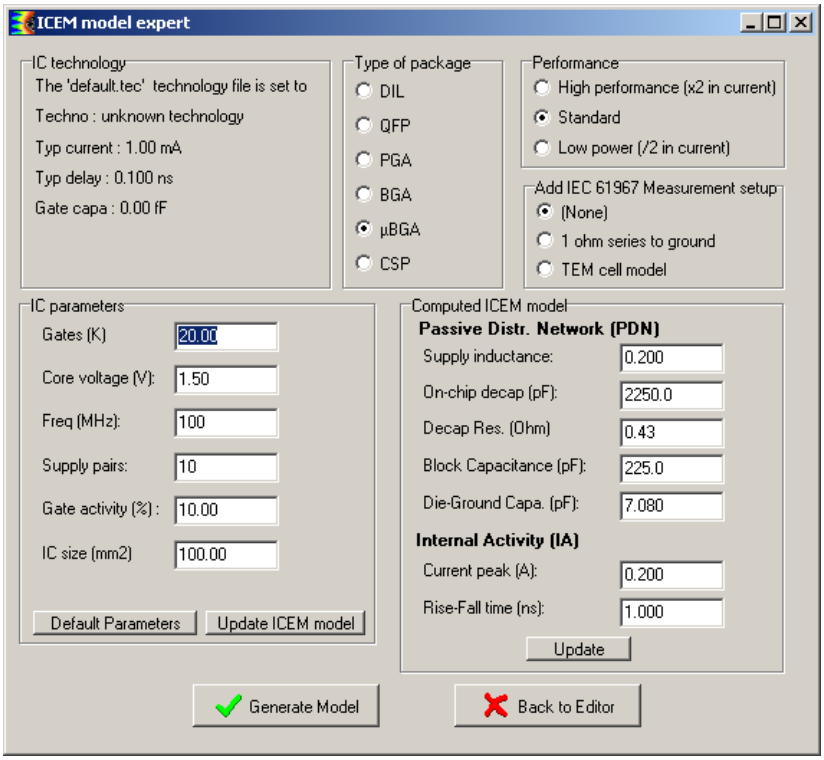


Figure 5-21: The ICEM model generator and its user interface

The next menu, called "Type of package", selects the family of package, which has a direct impact on package inductance. The "performance" menu tunes the current peak (Ib) by increasing the peak current by 100% in "high speed" mode as compared to standard mode. In "low power" mode, the current is reduced by 50%. In the lower left corner, several parameters that have a direct impact on the ICEM model are given:

- The number of gates (20 Kgates in the example)
- The operating frequency (100 MHz)
- The supply pairs (Number of VDD/VSS pins, 10 by default)
- The % of switching activity in each active edge of the clock (10% proposed here)
- The IC size in mm (10x10 mm in this example)

The button "Update ICEM Model" updates the proposed values for the Passive Distribution Network and the Internal Activity. The button "Generate Model" creates a simple schematic diagram from these parameters (Fig. 5-22a). You may also add:

- A 1-Ω serial resistance on the ground path, associated with 50-Ω adaptation as defined in the IEC standard "1/150Ω conducted measurement method" [5-4]. A probe is placed at the location of the measurement system, usually a spectrum analyzer (Fig. 5-22b)
- A capacitance/inductance coupling with the septum of the TEM cell, associated with 50-Ω terminations, as defined in IEC standard "TEM radiated measurement method" [5-11]. A probe is placed at the location of the measurement system, usually a spectrum analyzer (Fig. 5-22c).

The computation of the ICEM elements is performed using the approximations described in the reference manual 11.1.20 – ICEM Model Expert.

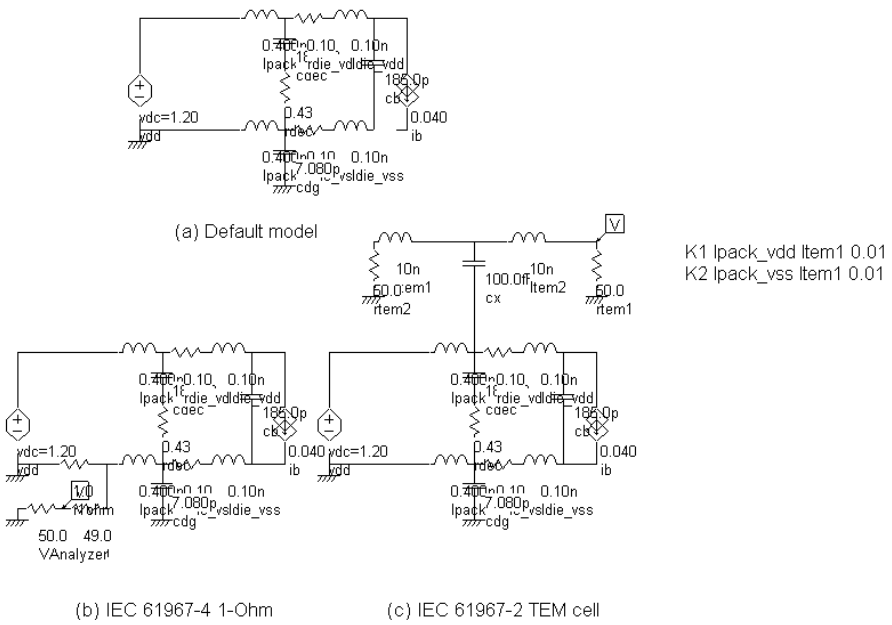


Figure 5-22: The ICEM model expert supports IEC 61967 "1/150Ω" and "TEM" standards

5.6.2 ICEM Model Expert – Application to TC1796

We illustrate the tool usage on the Infineon TriCore case study [5-12], an advanced 32-bit microcontroller dedicated to automotive applications. Simulations have been performed in advanced phase using the ICEM model expert, based only on the component data sheet [5-13] information and the IBIS model provided by Infineon.

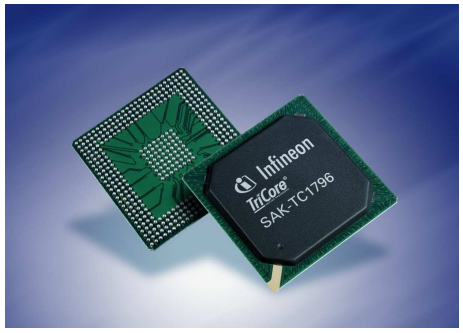


Figure 5-23: The 32-bit microcontroller TriCore TC1796 from Infineon [5-13]

5.6.2.1 IC reconstruction from IBIS

Click "File" → "Load IBIS file" and select "case_study\tricore\infineon_tc1796_v2.ibs". Click the item "Infos" to get general information about the component. Figure 5-24 describes the IBIS interface after opening the IBIS file and the general information of the file. Figure 5-25-a and b presents 2D and 3D views of the reconstructed package from IBIS file. We notice that the component has 50 "POWER" pins, and 66 "GND" pins.

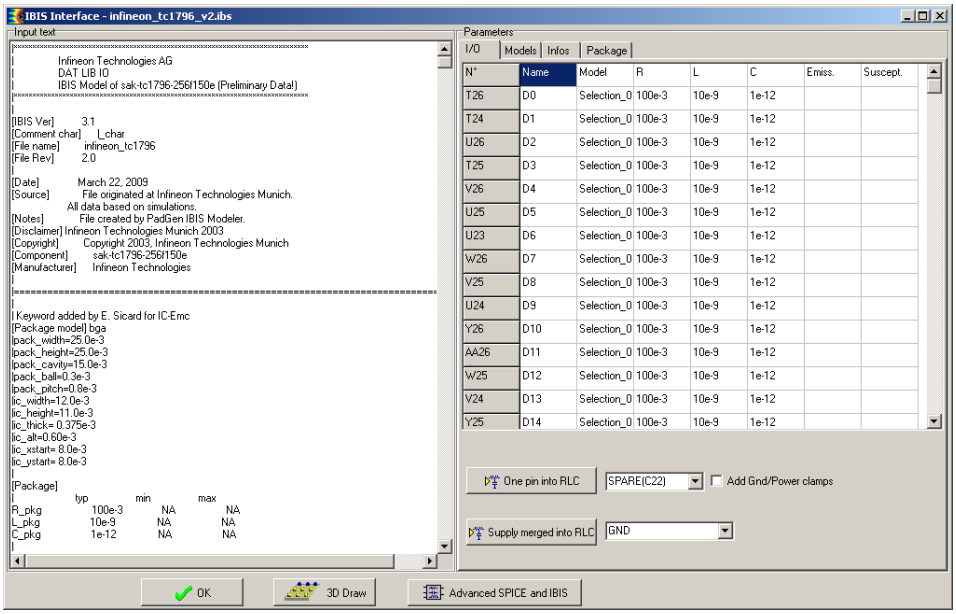
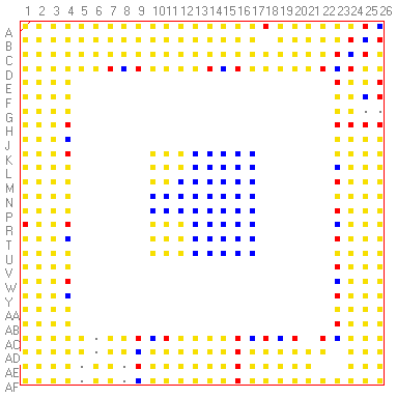
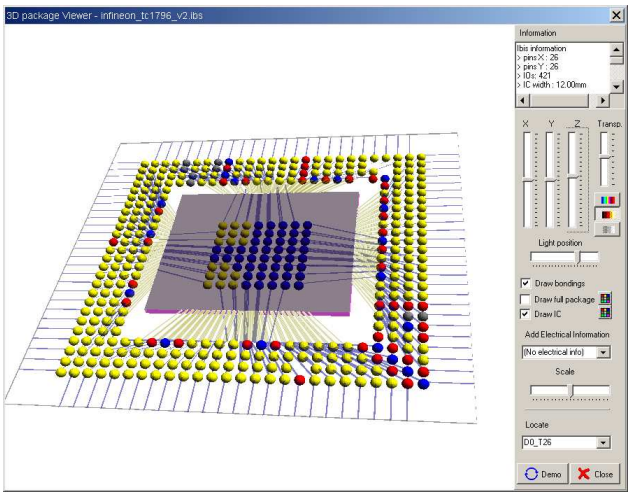


Figure 5-24: Downloading the TriCore TC1796 IBIS file (case_study\tricore\infineon_tc1796_v2.ibs)



(a) 2D-view

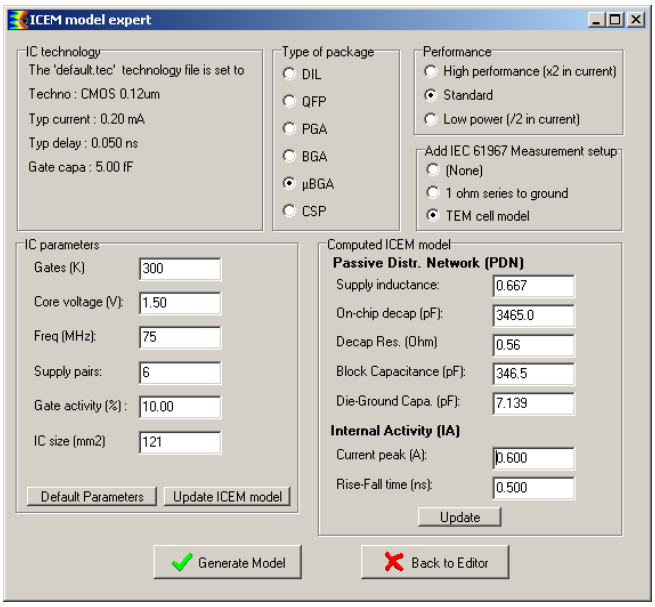


(b) 3D-view

Figure 5-25: 2D and 3D view of the TriCore TC1796 based on the IBIS file information (case_study\tricore\infineon_tc1796_v2.ibs)

5.6.2.2 ICEM Expert Parameters

Before launching ICEM Model Expert, load the technological parameters. The Tricore is designed in CMOS 0.12 µm technology. Click on File → Select technology, and open the file Lib\cmos012.tec. The parameters used to define the TriCore component in the ICEM model expert interface are listed in table 5-8. Most parameters are unconfirmed by the foundry, except the voltage supply, and number of supply pairs. Click "Generate Model" to create automatically the schematic diagram corresponding to the given parameters (Fig. 5-26). The default name is « example.SCH », use « File → Save As » to save the schematic diagram, for example as « TriCore_core_tem.sch ».



Parameter	Value	Description
Technology	Cmos012.tec	CMOS 0.12µm technology, 0.2 mA/gate peak current (unconfirmed).
Gates (K)	300	The TriCore core complexity is estimated to 300 K Gates (unconfirmed, can be tuned)
Core Voltage (V)	1.5	The logic core is supplied by 1.5V external voltage source (data-sheet)
Freq (MHz) :	150 - 75 MHz	The CPU clock of the Tricore operates at 150 MHz, with a multi-phase system (data sheet), while the peripherals and the external memory bus operates at 75 MHz
Supply pairs	58	The component has 50 "POWER" pins, and 66 "GND" pins ("Infos" in IBIS windows). We approximate to 58 pairs.
Gate activity (%)	10	At each clock edge, only 10% of the gates switch (unconfirmed, can be modified).
IC size (mm^2)	69	(information from a PDF description of the TriCore from Infineon)
Type of package	µBGA	Package pitch is 0.8mm, package ball diameter is 300µm (information from data sheet)
Performance	Standard	Neither very high speed (PC, servers) nor very consumption (mobile phones).
IEC 61 967 measurement standard	TEM Cell	Measurements provided by Infineon concern TEM cell measurements

Table 5-8 : TriCore parameters used in the ICEM model expert

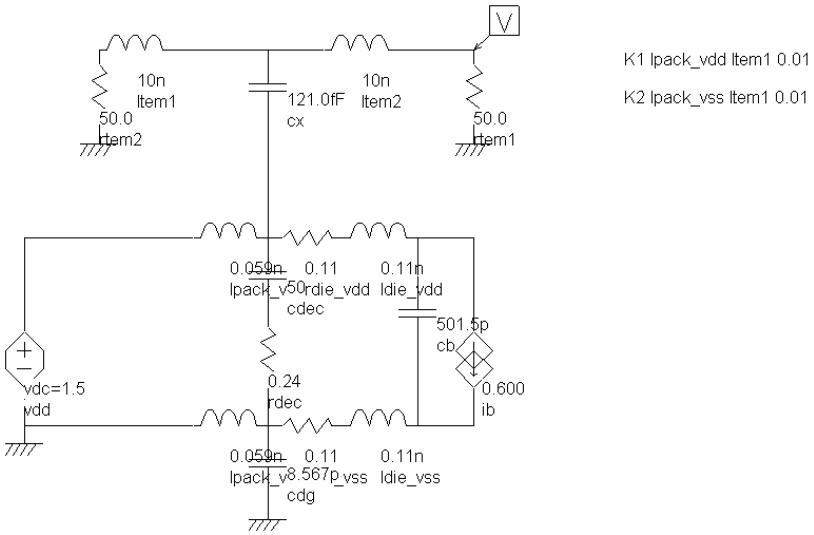


Figure 5-26: Schematic diagram generated by the ICEM model expert, ready for simulation

5.6.2.3 Comparison with TEM measurements

The IC manufacturer has published [5-14] TEM-cell measurements of the component, with two setups: one with core only, the second one with IOs.
Generate the SPICE file, execute the CIR file with WinSpice, and click “Emission vs. Frequency”. Click “Add Measurements” and select “case_study\Tricore\ TriCore_core_tem.tab” . The file “TriCore_tem_core.tab” includes the envelop of the TEM cell measurements performed on the TriCore, core alone, without any IO activity. The comparison with measurements is given in Fig. 5-27. It can be seen that the noise is overestimated by the default model.

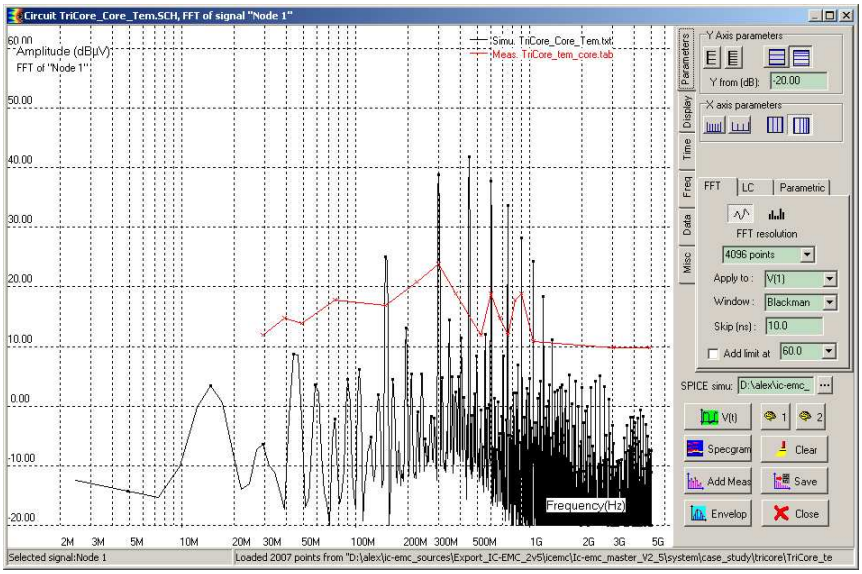


Figure 5-27: Comparison between the model generated by the ICEM model expert and real-case TEM measurements (case_study\Tricore\TriCore_core_tem.tab)

The model needs to be tuned to match the measurements. Possible actions are listed in table 5-9. The new simulations performed with WinSpice on the tuned model show some reasonable correlation as shown in figure 5-28, even if simulations are a little higher than measurements for almost all harmonics.

Decrease inductive coupling	K1 Lpack_vdd Item1 0.01 L2 Lpack_vss Item1 0.01	Default value is 0.01, equal to 1% coupling. This situation corresponds to one single lead. We may use K=0.001 (coupling of 0.1%) because the supply lines are routed in all directions and do not couple strongly with the septum
Increase on-chip decoupling	Cdec → 20 nF	The EMC design experts have increased the on-chip decoupling capacitance (information confirmed by Infineon) to 20 nF
Decrease peak current	Ib > I2 → 0.3 mA	The peak current might be less than expected, due to the use of low-power technology
Decrease current peak frequency to 75 MHz	Ib > Period → Increase to 13.33 ns (75 MHz)	Given a 75 MHz clock, we assume two equal current peaks, one at the rise edge, one at the fall edge, so that Ib frequency is 150 MHz. If we are in a 2-phase or 4-phase system, the main peak might appear at 75 MHz rate or even 37.5 MHz rate.

Table 5-9 : Possible tuning of the ICEM model and associated justifications

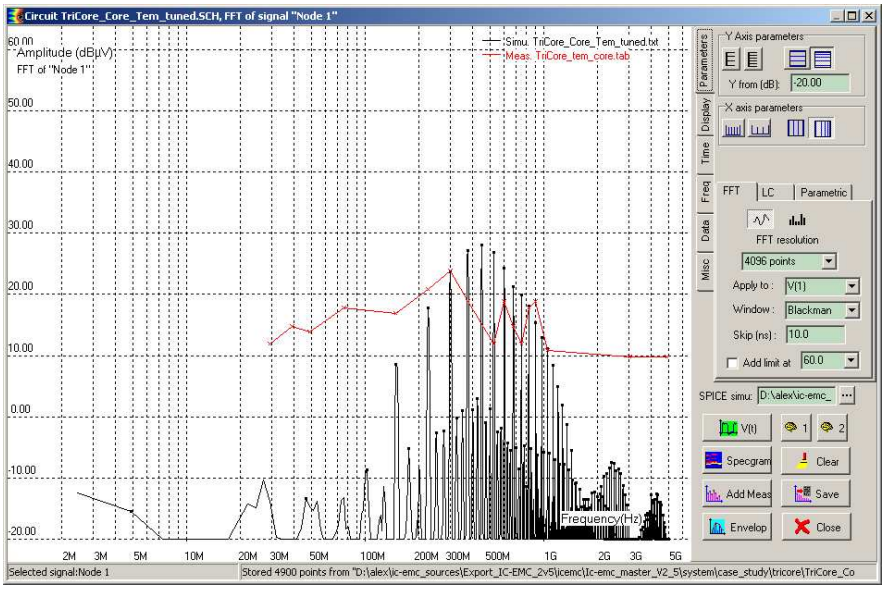


Figure 5-28: Comparison between the tuned model and real-case TEM measurements (case_study\Tricore\TriCore_core_tem_tuned.tab)

5.7 Summary

In this chapter, the flow for emission simulation with IC-EMC has been presented. The emission prediction is based on SPICE transient simulation followed by FFT algorithm done by IC-EMC. Several comparisons between simulation and measurement for conducted and radiated emission have been presented. Measurement results were associated to IC emission IEC-61967 standards, such as 1 Ω/150 Ω probe method and TEM cell method.

Accurately predicting the electromagnetic emission of a circuit is a difficult task as emission depends on numerous and complex elements such as the circuit activity, the circuit power supply network, the PCB routing… Timely simulation and layout-related confidentiality issues reinforces the need for IC macromodels. This chapter has put the emphasis in the Integrated Circuit Emission Model (ICEM) approach, illustrated on some microcontroller examples. The description of an original tool called ICEM Model Expert has also been given. From basic technological information of a circuit, such as the typical current activity, the typical gate delay…, this tool is able to build immediately a first-order ICEM model. This tool gives an instant estimation of conducted and radiated emission level from minimum circuit parameters.

5.8 References

[5-1] IEC61967-1 part 1, " Integrated Circuits, Measurement of Electromagnetic Emission, 150 KHz – 1 GHz: General and Definitions ", International Electrotechnical Commission, Geneva, Switzerland, March 2002

[5-2] IEC62433-2, "Models of Integrated Circuits for EMI behavioral simulation – ICEM-CE, ICEM Conducted Emission Model", International Electrotechnical Commission, Geneva, Switzerland, 2006

[5-3] IEC62404, "Logic Digital Integrated Circuits – Specification for I/O Interface Model for Integrated Circuits (IMIC version 1.3)", International Electrotechnical Commission, Geneva, Switzerland, 2007

[5-4] IEC 61967-4, "Methods of Conducted Emission – 1 Ω / 150 Ω Method", International Electrotechnical Commission, Geneva, Switzerland, March 2002

[5-5] IEC 62014-3, « Models of Integrated Circuits for EMI Behavioral Simulation », IEC standard, November 2004

[5-6] IEC62433-1, "EMC IC Modeling – Part 1: General Modeling Framework", International Electrotechnical Commission, Geneva, Switzerland, 2006

[5-7] The ICEM cookbook is available on line at http://www.ic-emc.org

[5-8] A. Boyer, S. Bendhia, E. Sicard, "Characterization of the Electromagnetic Susceptibility of Integrated Circuits using a Near Field Scan", Electronic Letters, IEE Society, 2007

[5-9] The PDF documentation of WinSPICE is available at www.winspice.com

[5-10] B. Vrignon, S. Bendhia, L. Courau, E. Sicard, "CESAME: a Test Chip for the Validation of a parasitic Emission Prediction Flow in 0.18 µm CMOS Technology", 2004 International Symposium on Electromagnetic Compatibility, 9-13 August 2004, pp 372-376, vol. 2

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[5-12] www.infineon.com Advanced 32-bit TriCore-based Microcontrollers for Automotive Embedded Control

[5-13] "TriCore 2 - 32-bit Unified Processor Core v2.0 Architecture", Architecture Manual (PDF on line, www.infineon.com), Edition 2006, Infineon Technologies AG, D-81541 München, Germany

[5-14] L. Bouhouch, S. Bendhia, E. Sicard and T. Steinecke. "Prediction of the radiated emission of an 32 bits Microcontroller". 15th European Microelectronics and Packaging Conference & Exhibition (IMAPS Brugge 2005), Brugge, Belgium, June 12-15, 2005, http://www.imapsbrugge.be/

5.9 Exercises

1. Exercise 1: Effects of parasitic inductance

To predict parasitic emission of digital core of integrated circuits, macro-modelling as ICEM model (IEC 62433) is often used, as it features accurate predictions while requiring a low complexity model. The internal activity of the digital core is usually descried using one or a reduced number of equivalent current sources, while the power distribution network is modelled by R, L, C elements.
IC-EMC provides a tool called ICEM model expert (Tools/ICEM model expert) which helps generating ICEM model of a digital circuit based on basic technological information. Let's consider a 16 bit microcontroller with the following parameters:

Technology	0.12 µm
Core supply voltage	1.2 V
Bus clock frequency	20 MHz
Number of gates	100 K
Gate activity	15 %
IC size	15 mm²
Package	QFP
number of core supply pairs	1
Performance	Standard
Emission measurement	0.1 ohm

The circuit is mounted on an "ideal" board, i.e. the power supply reference is supposed constant anywhere on the board.

1. Use the tool ICEM model expert to generate the ICEM model of the microcontroller core. Simulate the external conducted emission through a 0.1 Ω probe (the original 1 Ω probe has been modified to reduce the voltage drop across the 1 Ω resistor). Deduce the ground return current induced by the circuit activity.

2. Simulate the IC internal power supply and ground voltage bounce. What is the origin of the internal voltage bounce?

3. Do you think that the simulated noise is acceptable?

4. With the equation $V_L = L\frac{di}{dt}$ where V_L is the voltage drop across an inductance, compute the theoretical internal voltage drop. Is the theoretical result in accordance with the simulated one?

5. Propose a solution to reduce the internal power supply and ground voltage bounce. The design target is to reduce the internal voltage bounce amplitude under 10 % of the power supply voltage. Is it physically possible?

6. What is the effect of the previous solution on the external conducted emission?

2. Exercise 2: External decoupling (1)

The microcontroller described in the first exercise is reused. In order to reduce the conducted emission, external decoupling capacitors are placed all around the component. In this exercise, the parasitic effect of the board is neglected. Power supply and ground planes are supposed to be equipotential.

1. A conventional 100 nF ceramic capacitor is added between the power supply and the ground pin of the circuit. Be careful, the 0.1 Ω must not be placed between the circuit and the capacitor. Simulate the conducted emission. What is the effect on the conducted emission level? Why? Do you think that this result is realistic?

2. A real model of SMD capacitor is used. The capacitor model includes a serial 0.5 nH inductor (ESL) and a 100 mΩ resistor (ESR). Is the decoupling capacitor still so efficient? Compute the noise reduction for the five first harmonics.

3. Plot the impedance profile of the capacitor. Conclude about the limits of the decoupling capacitance efficiency.

4. Add an additional 10 nF capacitor in parallel with the 100 nF capacitor. Use the same ESR and ESL values. Simulate the conducted emission. Does this new capacitor contribute to reduce the noise? If yes, which harmonics have been reduced? Plot the impedance profile of both capacitors in parallel. Conclude about the effect of this new capacitor.

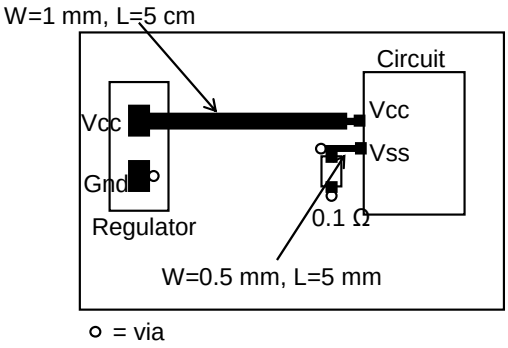
5. Try smaller capacitance value for the second decoupling capacitor (for example 1 nF and 100 pF). Is it useful to reduce the capacitance value?

3. Exercise 3: External decoupling (2)

The circuit described in exercise 1 is mounted on a two layers printed circuit board. The following schematic describes the top layer of the PCB, where the components are mounted. The bottom side is a full ground plane. The characteristics of the PCB are:

- substrate = FR4
- Thickness of the substrate = 1.6 mm

All the components are surface mounted devices. The schematic describes the connection of Vdd and Vss pins of the circuit to the power supply and ground references assured by a regulator. These references are supposed ideal. A 0.1 Ω resistor is added between the Vss pin of the circuit and the board ground plane.



1. Build the equivalent model of the circuit (use Tools/ICEM model expert) and the PCB (use Tools/Interconnect parameters). Simulate the conducted noise.

2. Place an ideal capacitor at different location of the power supply track. The decoupling capacitor is connected between the Vss pin of the circuit and the 0.1 Ω probe. What is the best location for the placement of the decoupling capacitor for the conducted emission? And for the radiated emission?

3. What is the effect on the internal voltage bounce?

6 Near-field scanning

Near field scanning has been widely used to exhibit “hot spots” at the surface of integrated circuits and to guide IC designers for reducing the parasitic emission [6-1]. The near-field scan has two main interests for EMC of ICs. First, a near-field scan performed at a short distance from the IC surface ensures the localization of current flowing without any contact (and thus a minimal intrusion of the measurement system). It provides valuable information about source for radiated emissions, parasitic coupling between separated blocks (e.g. due to substrate coupling), or near-field coupling or crosstalk between neighbour blocks. Secondly, the characterization of electromagnetic emission in the near-field area allows a prediction of the far-field emission of the circuit.
This chapter is dedicated to the prediction of the emission of integrated circuits in near-field area. The link between electrical macro-models such as ICEM and the near-field scanned information is investigated in this paragraph.
In previous chapters, we obtained good correlations between measured and simulated spectrum for the CESAME test chip in conducted and radiated modes. From these bases, our goal is to predict the near-magnetic field using the same model. To predict magnetic field, we rely on IC electrical models and package geometry to locate radiated elements.

6.1 Near field/Far field

Any conductor crossed by a variable current or pulsed by a voltage across its ends acts as an antenna. At PCB level, any track and especially the ones that form current loop can radiate electromagnetic (EM) waves. At circuit level, package leads and bonding wires are considered as long conductors and may be the cause of radiated energy (Fig. 6-1).

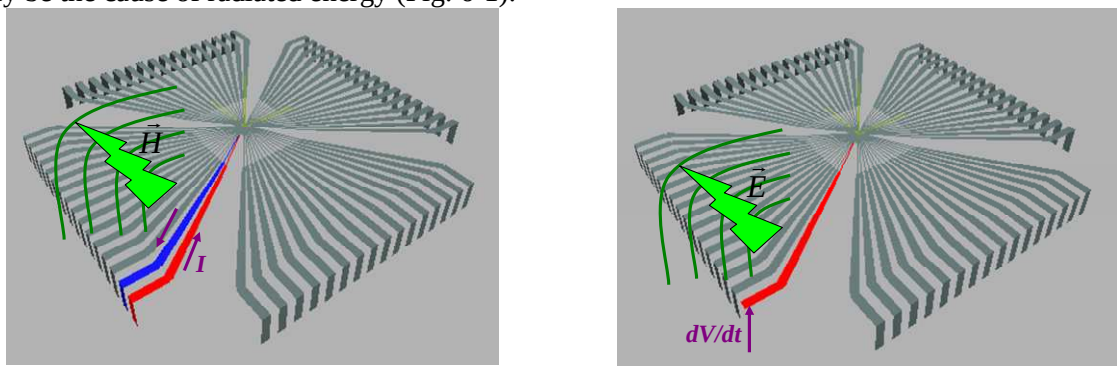


Figure 6-1: Radiation mechanisms at package level – Magnetic field (on the left) and electric field (on the right)

The radiation produced by any antenna can be divided in three domains (Fig. 6-2):

- The near field or Rayleigh area that surrounds the antenna. In this area, there is some reactive energy exchange between the antenna and its near environment. The plane wave is not formed.
- The Fresnel area which is an intermediate area between near field and far field radiation areas.
- The far field radiation where the electric and magnetic components of the EM fields form a plane wave. The far field area is located far from the antenna.

The limit between near field and far field corresponds to a change in the energy flow. The limit is reached when the dimension of the source antenna is short compared to the distance to the antenna. The value of this limit depends strongly on the wavelength λ of the considered radiation and the geometry of the antenna. For a short wire antenna, the limit R between near field and far field radiation area can be approximated by equation 6-1.

$$R \approx \frac{\lambda}{2\pi} = 0.16\lambda \qquad \text{Equ. 6-1}$$

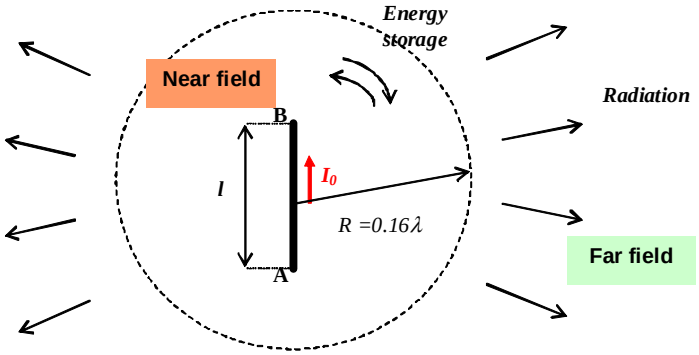


Figure 6-2: Reactive vs. Radiated energy flow or limit between near field and far field radiation area

As the plane wave is not formed in the near field area, many components of EM fields exist. Equations 6-2 to 6-4 give formulation for all electric field components and equations 6-5 to 6-7 for all magnetic field components in the case of a short wire crossed by a sinusoidal current, supposed constant along the wire (fig. 6-3) [6-2].

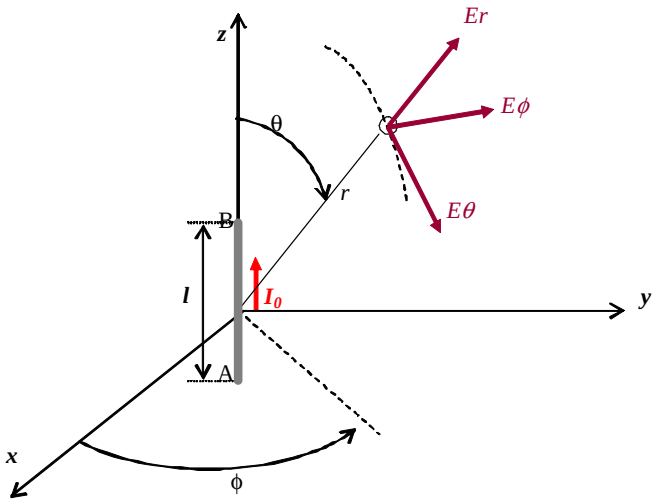


Figure 6-3: Short wire radiation

$$E_r = \frac{2I_0 l}{4\pi}\eta\beta^2 \cos\theta\left(\frac{1}{\beta^2 r^2} - j\frac{1}{\beta^3 r^3}\right)e^{j(\varpi\omega t-\beta r)} \qquad \text{Equ. 6-2}$$

$$E_\theta = \frac{I_0 l}{4\pi}\eta\beta^2 \sin\theta\left(\frac{j}{\beta r} + \frac{1}{\beta^2 r^2} - \frac{j}{\beta^3 r^3}\right)e^{j(\varpi\omega t-\beta r)} \qquad \text{Equ. 6-3}$$

$$E_\phi = 0 \qquad \text{Equ. 6-4}$$

$$H_r = 0 \qquad \text{Equ. 6-5}$$

$$H_\theta = 0 \qquad \text{Equ. 6-6}$$

$$H_\phi = \frac{2I_0 l}{4\pi}\eta\beta^2 \sin\theta\left(\frac{j}{\beta r} + \frac{1}{\beta^2 r^2}\right)e^{j(\varpi\omega t-\beta r)} \qquad \text{Equ. 6-7}$$

where:

r=distance from dipole center to point (m)
ϕ=angle in (x,y) plane (radian)
φ=angle from z axis (radian)
i=current from A to B (A)
f is the current frequency of the current (Hz)
c=speed light = $3x10^8$ m/s
η=wave impedance = 377 Ω

Propagation constant $\beta = \frac{\omega}{c} = \frac{2\pi}{\lambda}$

Wavelength $\lambda = \frac{c}{f}$

Pulsation $\omega = 2\pi f$

Each component of E and H fields has some$1/r^2$ or $1/r^3$ terms. These terms are very strong in the near field radiation area but decrease very rapidly when distance from the antenna increases (fig. 6-4). Far from the antenna, $1/r^2$ or $1/r^3$ terms can be neglected and only 1/r terms can be kept, which leads to only two components (Equ. 6-8 and 6-9). These two components form the plane wave in the far field area.

$$E_\theta = j30I_0\beta l\frac{e^{j(\varpi\omega t-\beta r)}}{4\pi r}\sin\theta \qquad \textit{Equ. 6-8}$$

$$H_\phi = jI_0\beta l\frac{e^{j(\varpi\omega t-\beta r)}}{4\pi r}\sin\theta \qquad \textit{Equ. 6-9}$$

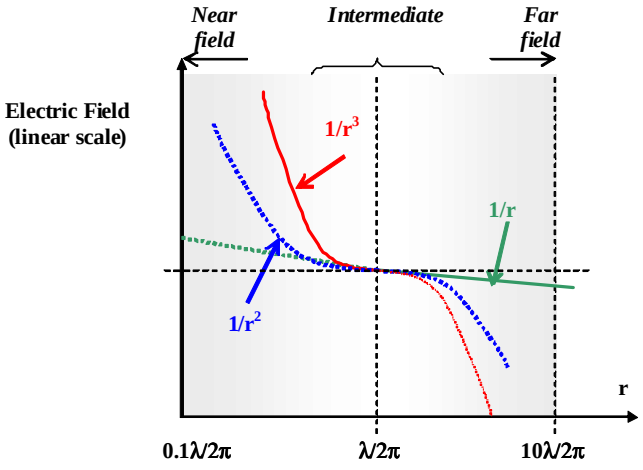


Figure 6-4: Electric field components in near and far field radiation area

6.2 Near-field scanning method

The measurement of the electric or magnetic components in the near field is interesting for EMC of ICs because it helps to locate transient current circulation as well as strong voltage variations. Indeed, at very short distance from a conductor, it is possible to separate the respective contributions of each part of this conductor. As distance from the conductor increases, all of these contributions superimpose and only the global radiation from the conductor can be measured.
A near field scan measurement method is described in the international standard IEC 61967-3 [6-3]. It consists in placing a miniature antenna, also called near-field probe, at very short distance from a

device under test and measuring the signal induced by the coupled field [6-4]. The near field probe is usually a simple loop or wire antenna to measure respectively one component of magnetic or electric field [6-5]. The probe is moved at different position above the surface of the device under test in order to produce cartographies or scans of the coupled field. The principles of magnetic near scan measurement are illustrated in Fig. 6-5. A magnetic field probe which consists in a small loop formed at the extremity of a coaxial cable senses the magnetic field produced by all the conductor of the circuit (Fig. 6-6).

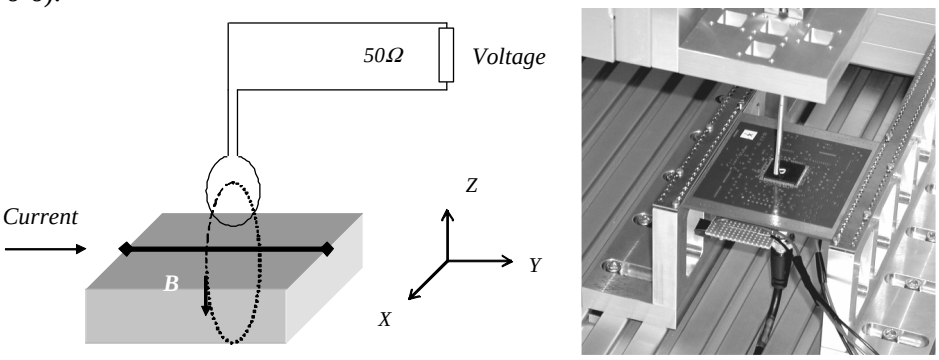


Figure 6-5 : Principles for near field scan of the magnetic field radiated by a circuit

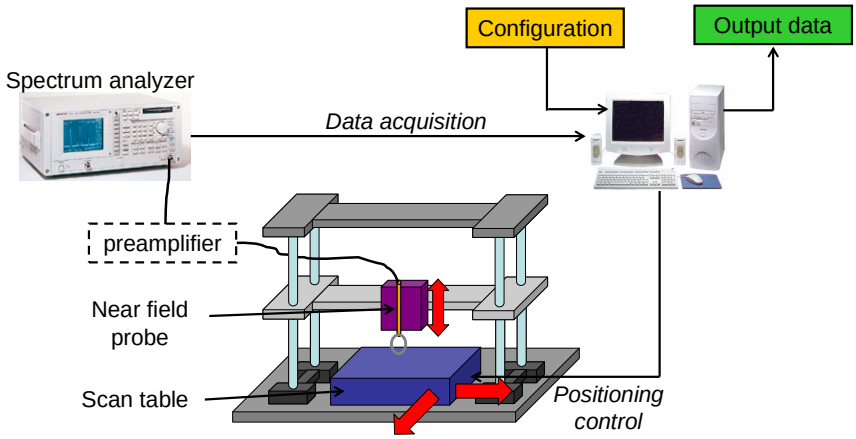


Figure 6-6 : Description of a usual near field scan test bench [6-6]

Measurement of near field is quite complex, as it requires an accurate positioning of the near-field probe over a device under test and an iterative procedure for signal acquisition with varying frequency and position in space, as described in the flow of Fig. 6-7.

6.3 Near-field Prediction

Various methods exist to compute EM fields produced by conductor. Three-dimensional full wave simulators are based on numerical methods that can adapt to any conductor geometry. They are not only the most accurate but also the most time consuming methods. In contrast, methods based on analytical formulations or geometry simplifications are very fast but they are limited only to simple problems. The choice of an EM field solving method depends on the required accuracy level and the maximum simulation time. For example, at an early design phase, exact models can not be available and simple calculations are often required to set some design budget. Full wave simulations can only be performed at design end for optimization purposes.

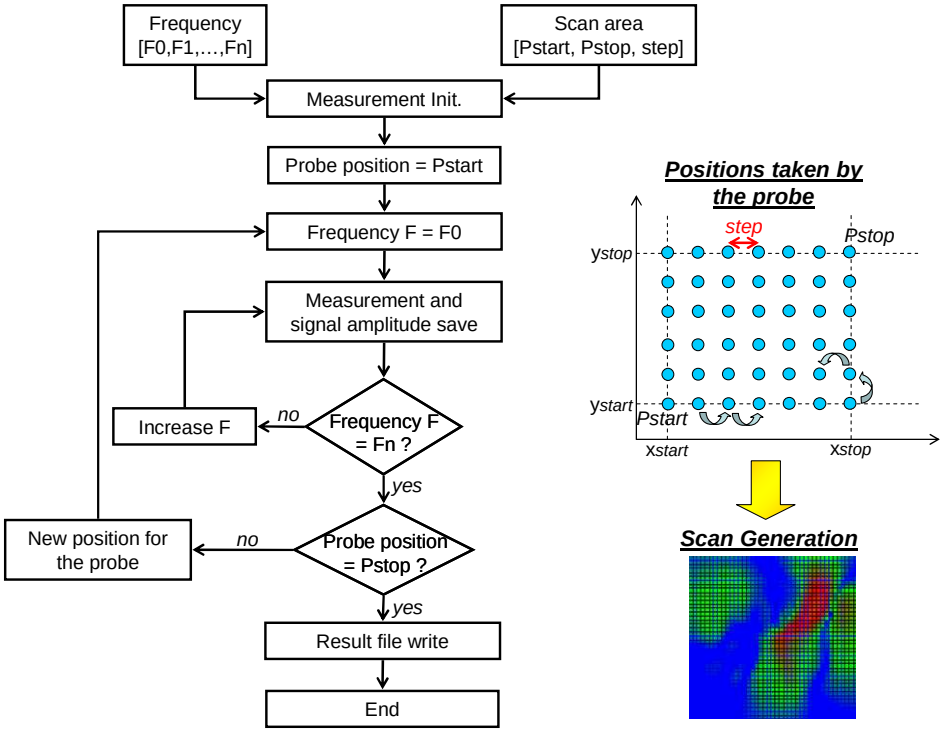


Figure 6-7 : Description of the near field scan measurement procedure

However, a full wave simulator is not the best approach to predict radiated emission from integrated circuits. Indeed, ICs produce strongly non-linear currents which can not be handled by full wave simulator. Co-simulation tools including electrical and EM simulators are required to simulate both non-linear responses and radiation of ICs. Figure 6-8 describes the general simulation flow of this type of tool. EM fields are extracted from voltages and currents crossing metal interconnects of ICs. At IC level, package leads and bonding wires are the largest interconnects. As most of electromagnetic solvers are based on frequency domain methods, FFT algorithm is required.

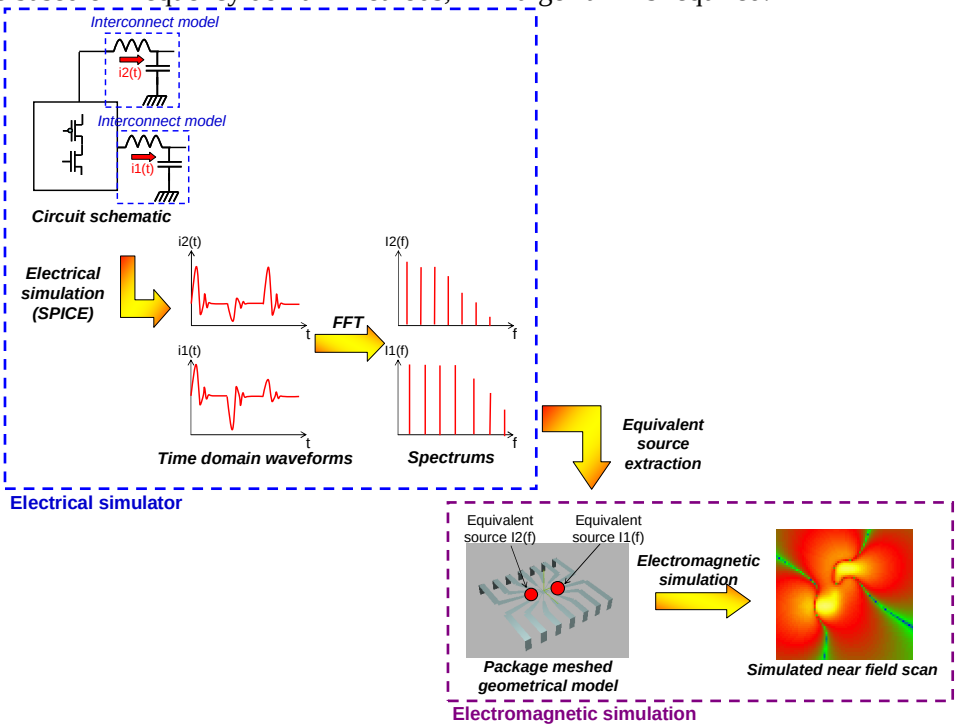


Figure 6-8 : General simulation flow for IC radiated emission prediction

For large circuits mounted in complex package and board, the use of transistor based netlist for IC modeling and full wave simulator become inefficient because of the over-complexity of models. Approximations are thus required to obtain results in a reasonable time. Approximations can affect electrical or electromagnetic models.
IC-EMC proposes a co-simulation method to estimate near field emission from ICs. Circuit simulations are handled by WinSPICE. An EM simulator is offered by IC-EMC to extract electrical and magnetic field at any point in (X,Y,Z) from WinSPICE simulations of the currents flowing through and the voltages across the radiated inductances, by means of some approximations concerning the package and electromagnetic field formulations. The general flow used to achieve a comparison between near-field measurement and simulated magnetic field emission is proposed in figure 6-9. The main novelty is the assumption that package leads used for supply and output signals are the main radiating elements [6-7].

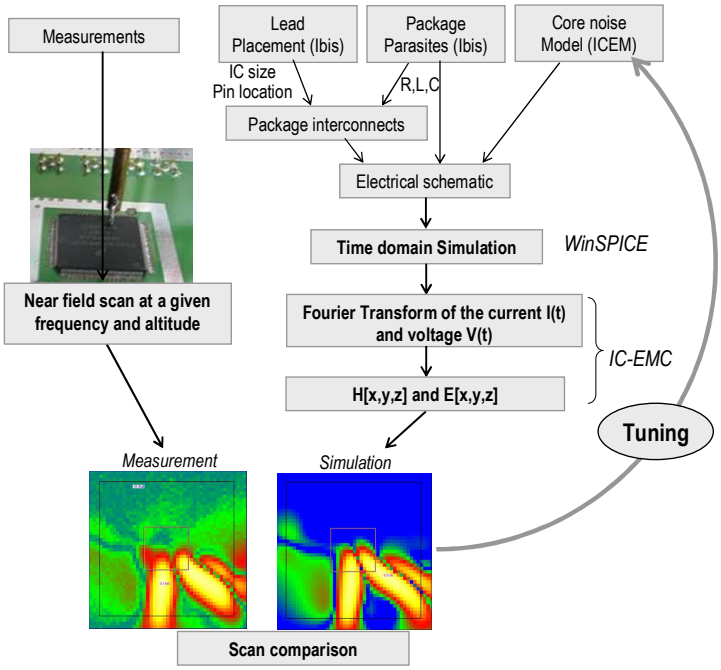


Figure 6-9 : Flow for comparing predicted and simulated magnetic field scans

6.3.1 Package modeling and geometrical reconstruction

At package level, leads and bonding wires are considered as the main radiated elements so that the package model is very important for the prediction of near field scan. As explained in the previous section, IC-EMC uses the current computed by WinSPICE to compute the resulting radiated emission. A link must be made between the current and the radiated elements. Two methods are used to model the radiating elements. In the first method, as the package leads and bonding wires are mainly inductive at low frequency, this link is made with the inductances which model package leads. These inductances called “radiating inductances” are classical inductances through which transient current flows, with attached geometrical coordinates. Simple geometrical models are considered for the package. Leads and bonding wires are modeled by one or several straight wires (Fig. 6-10).

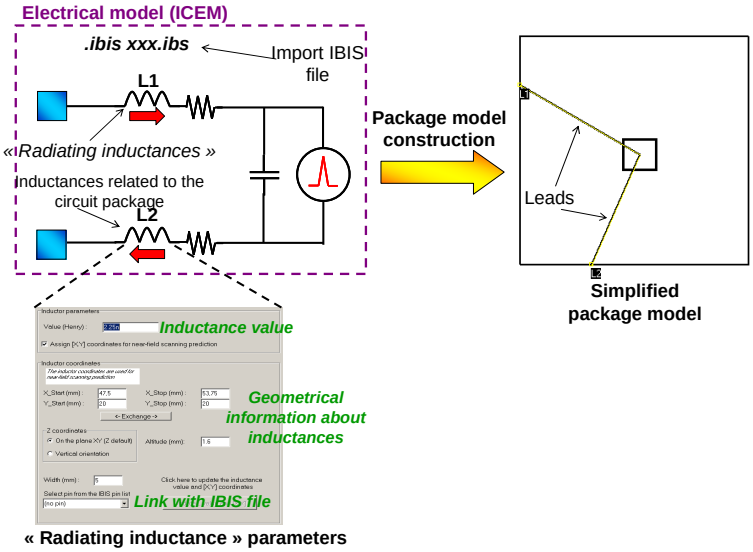


Figure 6-10 : Principles of simplified package model reconstruction and link to the electrical model through "radiating" inductances

This method assumes that the transient current circulates along electrically short interconnect, so that the "capacitive effect" of package interconnects can be neglected (i.e. charge storage). This assumption is valid until package interconnect length is less than λ/10 (quasi-static approximation). When package interconnects become electrically long, taking into account the "capacitive effect" of package interconnect become essential, especially for the prediction of electric field distribution in near-field. Indeed, a large part of electric field in near-field area is linked to charge storage, which cannot be modeled by inductance.

A more realistic electrical modeling approach consists in modeling interconnect by distributed RLC cells (see chapter 3 part 3 – Interconnect model). IC-EMC proposes a second method for a more accurate prediction of near-field emission based on a component called "Radiated Interconnect", available in the Symbol Palette  . Figure 6-11 presents the model of a small microstrip with the follwong parameters: width = 0.25 mm, thickness = 0.25 mm, height = 0.7 mm, length = 10 mm, epsr = 4.5. The electrical model is valid up to 1 GHz, so that a simple RLC π-cell is necessary to model the behaviour of this interconnect. Fig 6-11 shows the properties of this symbol: the equivalent resistance, inductance, capacitance of the RLC cell; the geometrical properties of the interconnect piece modeled by the RLC cell (the piece is assumed to be a straight line); and an authorization for near field scan simulation, i.e. the current flowing through the interconnect and stored charge will be computed and saved for near-field simulation.

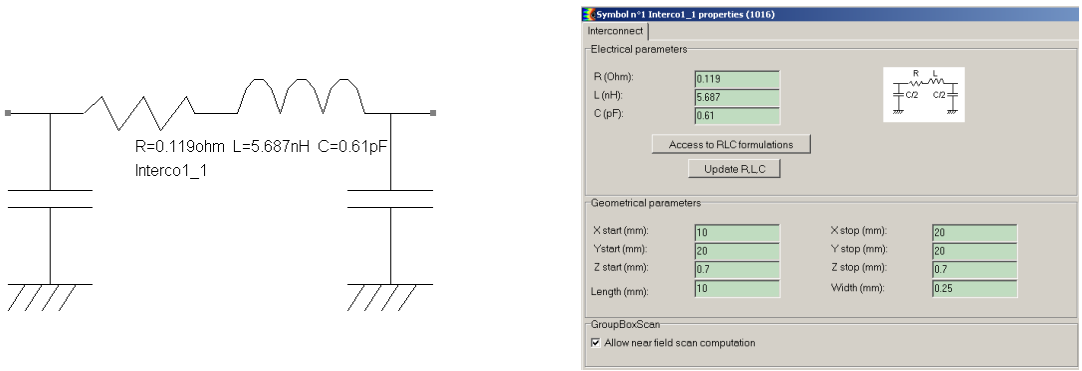
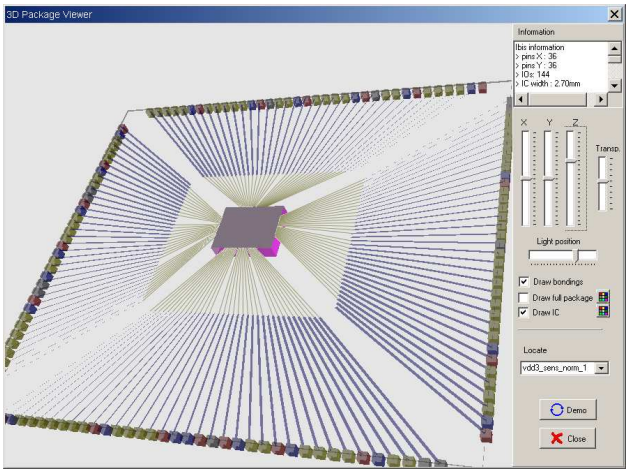


Figure 6-11 : Radiated interconnect symbol and properties (electrical, geometrical properties and near-field scan simulation authorization)

The geometrical information of “radiating inductances” can be entered manually or given by IBIS file. As described in chapter 4, IBIS provides some basic information about the package which are adapted to a simple geometrical representation. The package and die size information text are added in the [package model] section, in the IBIS file. The comment is mandatory to avoid parsing errors with conventional IBIS readers. However, IC-EMC can locate ‘|pack_’ and ‘|ic_’ keywords and get the relevant information. The 2D and 3D views of the package may then be reconstructed, as shown in fig. 6-12. (See chapter 4 section 4-3 or 11.1.17 for more information about package physical information included in IBIS file).




```
|
| Keywords added by E. Sicard for IC-EMC
|
[Package model] qfp
|pack_width=20.1e-3
|pack_height=20.1e-3
|ic_width= 2.7e-3
|ic_height= 2.5e-3
|ic_xstart= 9.2e-3
|ic_ystart= 9.2e-3
|pack_cavity=8.5e-3
|pack_pitch=0.5e-3
|pack_xstart=23.1e-3
|pack_ystart=24.1e-3
|ic_altitude=0.8e-3
```

Figure 6-12 : Physical parameters added to the IBIS model of CESAME to account for the package and die size (Cesame_v14.ibs)

6.3.2 Near-field Prediction Steps

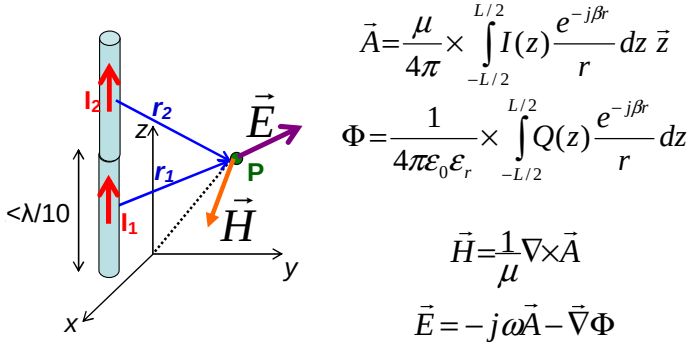
Assuming that the package bonding wires and leads are the main radiating elements, their associated current must be characterized, prior to magnetic field reconstruction (and also charge storage for electric field reconstruction). Therefore, the simulation steps are as follows:

1. The IBIS file is loaded, from which the pin list, package dimension and type are extracted
2. From the IBIS information, the package is reconstructed. Each lead is assigned a position in space.
3. Selected inductances (mainly supply and IO inductances) are assigned the corresponding space coordinates (or select radiated interconnects).
4. The analog time-domain simulation is performed to characterize all currents flowing in each declared package inductances.
5. The Fourier transform applied for each of these currents gives the magnitude I(f) for a frequency chosen for scanning.
6. Theoretical formulations are used to compute the sum of H and E contributions at each location of the space [x,y,z].

7. A post-processing displays the resulting magnetic field at the user-defined distance above the ground plane.

6.3.3 Near-field formulations

Formulations used by IC-EMC to compute electric and magnetic fields radiated by a package are based on the thin wire approximation. Each lead of a package is meshed in small elementary thin wire crossed by a current constant over all the lead. This assumption remain valid until the lead length is negligible in comparison to the wavelength (length < λ/10).
The electric and magnetic fields generated by of each elementary wire are calculated from the equations reported in figure 6-13. Parameters are the length of the current element *l*, the current amplitude *I0* in the element (A), and ω=2π.*f* (rad/s). The magnetic current at the observation point is the sum (in complex domain) of all elementary currents flowing in all leads.



$$\vec{A}=\frac{\mu}{4\pi}\times\int_{-L/2}^{L/2} I(z)\frac{e^{-j\beta r}}{r}dz\,\vec{z}$$

$$\Phi=\frac{1}{4\pi\varepsilon_0\varepsilon_r}\times\int_{-L/2}^{L/2} Q(z)\frac{e^{-j\beta r}}{r}dz$$

$$\vec{H}=\frac{1}{\mu}\nabla\times\vec{A}$$

$$\vec{E}=-j\omega\vec{A}-\vec{\nabla}\Phi$$

Figure 6-13 : Electric and magnetic field formulations with the thin wire approximation

If the package lead is longer than lambda/10 (where lambda is the wavelength of interest), the package is split into elementary dipoles as shown in figure 6-13. The software code has first been prototyped and validated under Scilab [6-8], and compared with a 3D field solver [6-9]. The electric and magnetic current at the observation point are the sum (in complex domain) of all elementary currents flowing in the package leads (Fig. 6-13).
In order to improve the accuracy of the near field prediction at short distance from the radiating source, the size of the conductor is also taken into account. Conductors associated to radiating inductances are assumed to be thin tracks characterized by a constant width. This geometry is valid for most conductor geometry found in electronic applications, such as PCB tracks or package leads.

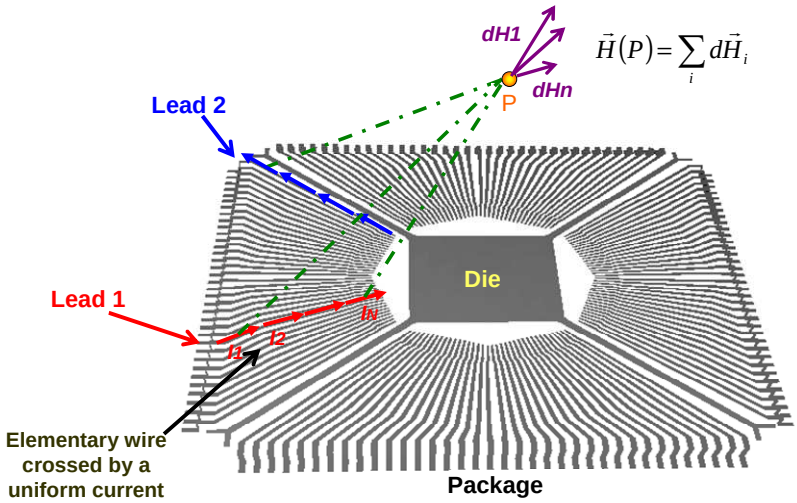


Figure 6-14 : Decomposition of package leads in elementary thin wires and contribution to the total electric and magnetic fields

6.3.4 Validation case – A 50 ohms microstrip line

The near field emission of a 50 ohms microstrip line is simulated with IC-EMC and an electromagnetic solver based on method of moments: FEKO [6-9]. A lumped model of the microstrip line is automatically generated with the tool "EMC → Interconnect Parameters". The geometrical parameters of the line section are reported in figure 6-15. The length of the line is 50 mm. Open the tool Interconnect Parameters, set the different parameters and click on the button "Apply y=f(x)" to compute the electrical characteristics of the line. Verify that the characteristic impedance of the line is close to 50 Ω. The model will be valid up to 1 GHz (field "Freq (GHz)". Finally, check the box "Near Field Analysis" and click on the button "SPICE Model" to generate the electrical schematic of the line. Figure 6-16 presents the generated schematic diagram.

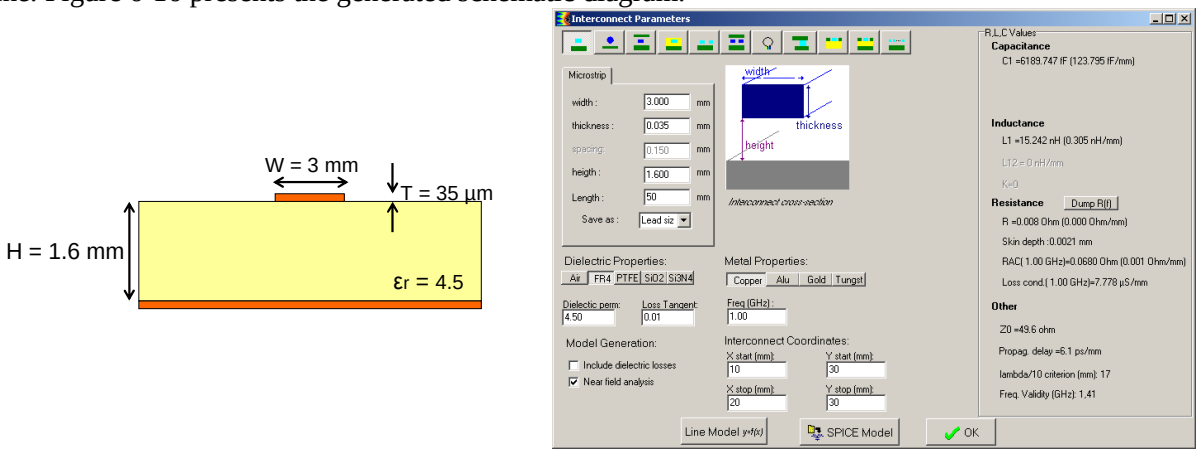


Figure 6-15 : Near field simulation validation case and automatic generation of an electrical model of a microstrip line

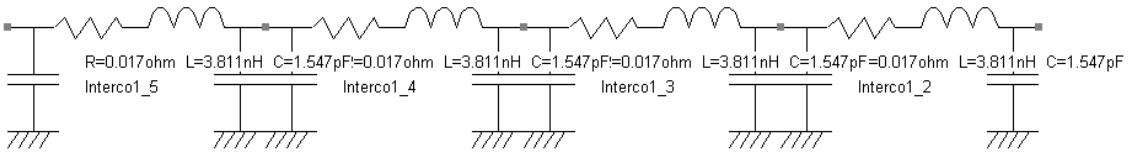
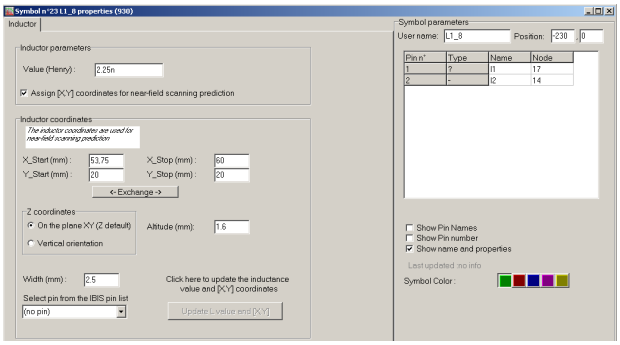


Figure 6-16 : Electrical lumped model of the microstrip line (near field\microstrip\microstrip50ohms.sch)

If you double click on radiated interconnects of the line, you can check that they are characterized by coordinates of the start and stop point, a direction and a width. Coordinates of each inductance are deduced from the information about length and λ/10 criterion at the maximum frequency of interest.



The microstrip line is fed by a signal generator through a coaxial connector placed on the ground plane side. The central connector has a radius of 0.6 mm and cross the substrate thickness. A 50 ohm loads is also placed on the ground plane side. The connection of the load to the line is ensured by a 0.6 mm radius connector.

6.3.4.1 Via Model

Two vias are used for interface the cable and one end of the microstrip line, and between the other end of the line and the load. A lumped model of the via is automatically generated with the tool "EMC → Interconnect Parameters". Enter the following characteristics for the via:

- via radius = 0.6 mm

- via thickness = 0.5 mm
- via height = 1.6 mm

Now, check the box “Inductances used for Near Field Analysis” and click twice on the button “SPICE Model” to generate the electrical model of both via, which is composed of one inductance and a serial resistor. Place this model at each terminal of the line.

Click on the each inductance of both vias and enter the coordinate X and Y of the terminal of the line: (10,30) and (60,30). The Z coordinates of the vias have been updated from information of Interconnect Parameters tool. Be sure that the orientation of both via is inverted to model correctly the circulation of the current through the line: the altitude of one via starts at 0 mm and stops at 1.6 mm, while the altitude of the other via starts at 1.6 mm and finishes at 0 mm. Finally, place a sinusoidal voltage generator at one side of the line and a 50 Ω load on the other side.

6.3.4.2 Simulation

The model is described in the file called “near field\microstrip\microstrip50ohms.sch”. The generator frequency is equal to 100 MHz and its amplitude is 1 V. Generate the SPICE netlist and then simulate it under WinSPICE. SPICE simulation provides transient profiles of current flowing through and voltages across the radiated inductances. These results are given in two separated files. If current profiles are written in a file called myfile.txt, charge information are written automatically in a file called myfile_Q.txt.
At the end of simulation, open the near field interface and set the scan altitude to 2.6 mm. This altitude is referenced to the ground, so the scan surface is located at 1 mm above the line. Check the box “Ground Plane at z = 0” to set a perfect ground plane under the line. Result file name should appear in the field “Input File”/”Use File”. Check the boxes “Simulate H field” and “Simulate E field” if you want to simulate either H field or E field or both.
The electromagnetic simulation is launched when the button “Simul. Scan” is pushed. The progression of the simulation is indicated at the bottom left of the screen. At the end of the simulation, select the component of the electric or magnetic field that you want to display in the list “Display Field”. Select the Y component of the magnetic field Hy. Figure 6-17 presents the displayed simulation result. The scan area is a 15 cm*15 cm surface above the line. The maximum value reaches 3.54 dBA/m right above the line. This simple simulation shows one of the interests of the measurement of near field emission: localizing the circulation of current.

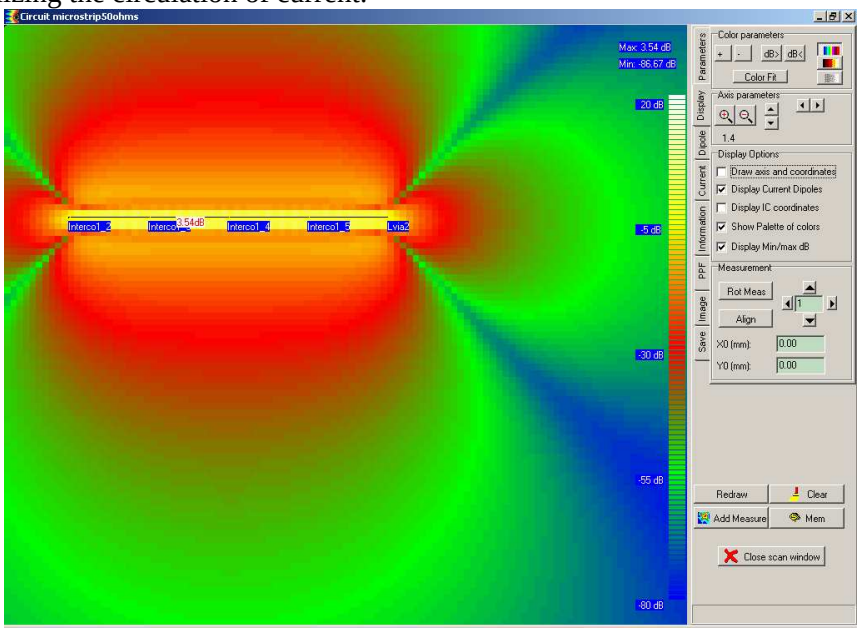


Figure 6-17 : Simulation with IC-EMC of the Hy above a 50 ohm microstrip line (near field\microstrip\microstrip50ohms.sch)

In order to validate the near field simulation done by IC-EMC, a 3D electromagnetic solver, FEKO [6-9] is used. This full wave solver is based on the method of moment. The same model is built, as shown on figure 6-18 (a). A near field scan simulation is done in the same condition and on the same scan area. Figure 6-18 (b) presents the simulated magnetic field Hy.

6.3.4.3 Comparing FEKO and IC-EMC

The maximum value provided by FEKO simulation is equal to 4.46 dBA/m. The magnetic field aspect as computed by FEKO (Fig. 6-18) is very similar to the one simulated with IC-EMC (Fig. 6-17). We propose an in-depth insight by comparing the simulated fields in a 2D graph. The magnetic field is computed along a line perpendicular to the line. In IC-EMC, click on "Save" field, select "Y" in Along Axis and choose 35 in the box "At coordinate of axis X (mm):". Then click on the button "2D graph" and a new window appears. Select the component of the field and click on the button "Add Measure". Figure 6-19 compares the simulation results of Hy computed by IC-EMC (on the right) and FEKO (on the left). An excellent correlation appears between the results provided by both simulator.

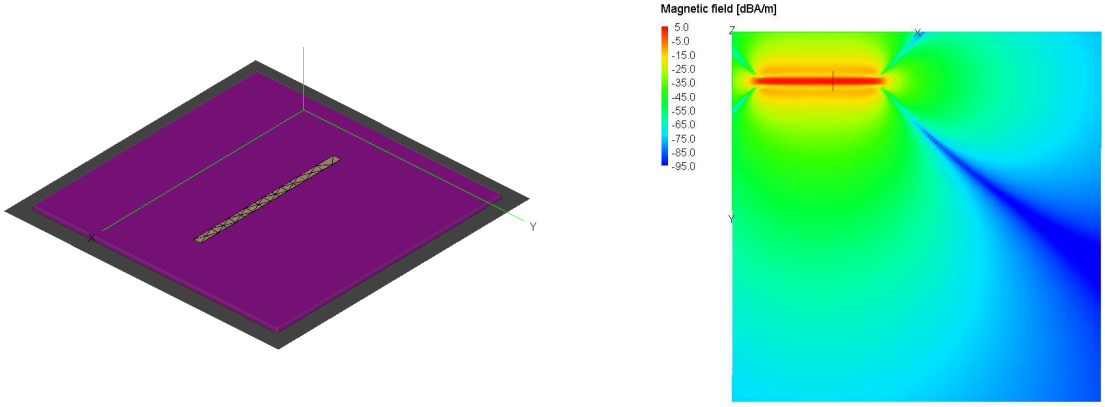
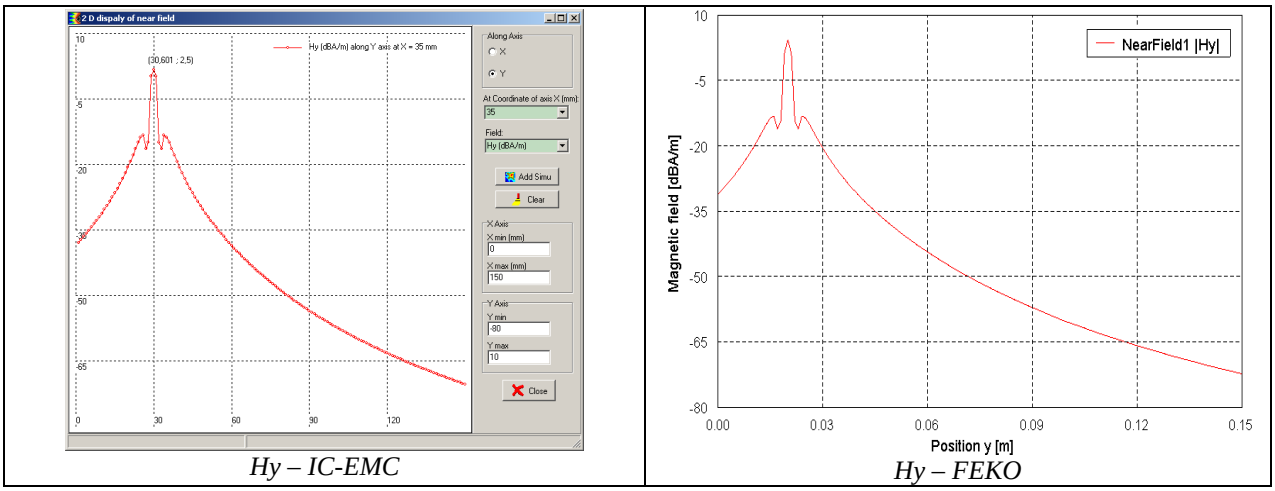


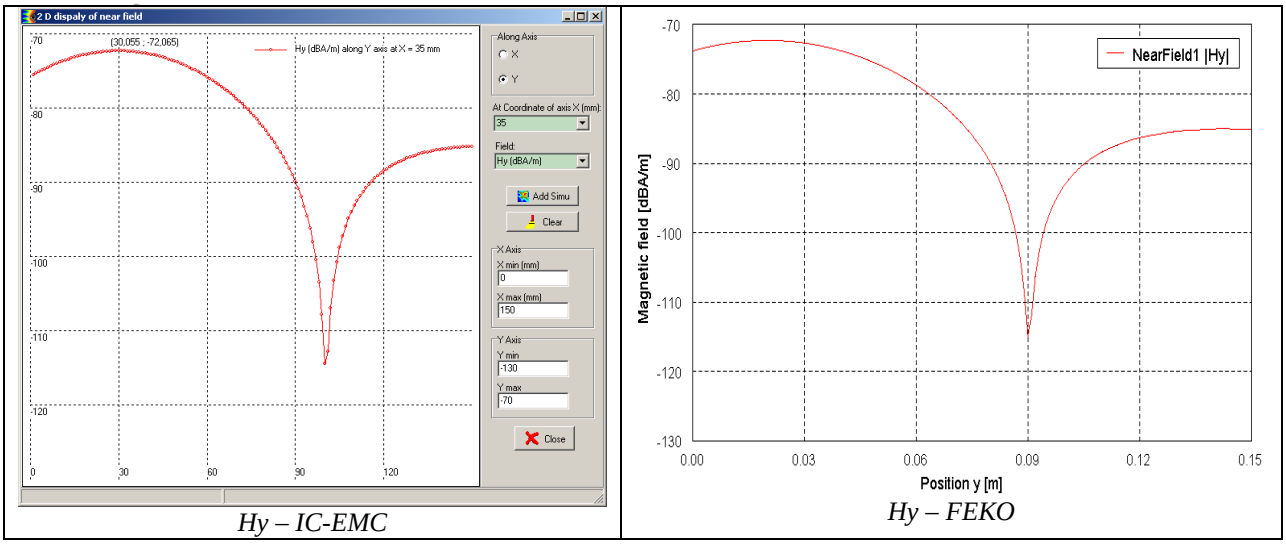
Figure 6-18(a): Geometrical model of the microstripline under FEKO – (b): Simulation with FEKO of the Hy above a 50 ohm microstrip line



Hy – IC-EMC *Hy – FEKO*

Figure 6-19 : Comparison of Hy field at h=1mm above the microstripline simulated with IC-EMC and FEKO (near field\microstrip\microstrip50ohms.sch)

A second comparison is done at higher altitude. In IC-EMC, change the scan altitude to 101.6 mm. The scan area is placed at 100 mm above the radiating inductances. Figure 6-20 presents the comparison. Once again, the correlation between the simulations done by both simulators is quite perfect.



Hy – IC-EMC *Hy – FEKO*

Figure 6-20 : Comparison of Hy field at h=100 mm above the microstripline simulated with IC-EMC and FEKO (near field\microstrip\microstrip50ohms.sch)

6.4 References

[6-1] K. P. Slattery, J. Neal, W. Cui, "Near Field Measurements of VLSI Devices, IEEE Transactions on Electromagnetic Compatibility, Vol. 41, no 4, 1999, pp 374-384

[6-2] C. R. Paul, "Introduction to Electromagnetic Compatibility", Wiley Interscience, ISBN 0-471-54927-4, 1992

[6-3] IEC 61967-3, "Methods of Radiated Emission – Surface Scan Method", Technical Specification, International Electrotechnical Commission, Geneva, Switzerland, March 2002

[6-4] K. Haelvoet, S. Criel, F. Dobbelaere, L. Martens, "Near-Field Scanner for the Accurate Characterization of Electromagnetic Fields in close Vicinity of Electronic Devices", IEEE Instrumentation and Measurement Technology Conference, Brussels, Belgium, June 4-6, 1996

[6-5] M. Kanda, "Standard Probes for Electromagnetic Field Measurements", IEEE Transactions on Antennas and Propagation, vol. 41, no 10, October 1993

[6-6] C. Labussière, C. Lochot, A. Boyer, " Characterization of the Radiation from a 16 bit Microcontroller by using miniature Near-Field Probes", EMC Compo 05, Munich, Germany, 29 – 31 November 2005, pp. 33 – 38

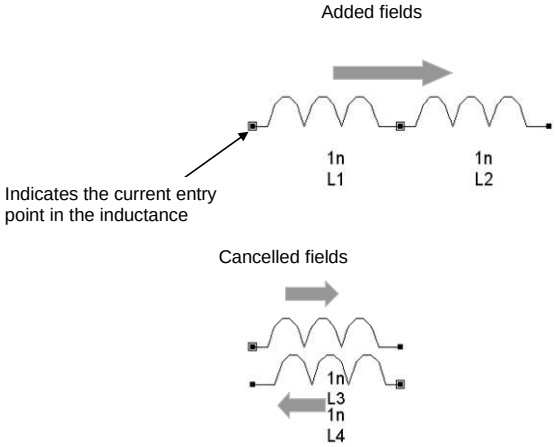
[6-7] S. Ben Dhia, M. Ramdani, E. Sicard, "EMC of ICs: Techniques for Low Emission and Susceptibility", Springer, USA, 2006, 474 p, ISBN 0-387-26600-3

[6-8] The SCILAB software can be downloaded from http://www.scilab.org

[6-9] More information about FEKO software at http://feko.info

6.5 Exercises

4. Exercise 1 – Magnetic field cancellation

Consider the following schematic diagram where two inductances are placed in or placed close and with opposite entry points (use the command **Edit → Flip Vertical** and select the desired component). The schematic is proposed in the file "near_field\exercises\field_cancellation.sch".	

Assign the following coordinates to the four inductances:

- L1: x0 = 30, y0 = 20, x1 = 50, y1 = 20
- L2: x0 = 50, y0 = 20, x1 = 70, y1 = 20
- L3: x0 = 40, y0 = 50, x1 = 60, y1 = 50
- L4: x0 = 60, y0 = 55, x1 = 40, y1 = 55

The interconnections modeled by these inductances are placed above a ground plane, the default altitude is set to 1 mm. The interconnect width is set to 1 mm. Connect these inductances to a sinusoidal voltage source and to a 100 ohms resistive load. Give the same characteristics to each line.
Simulate the magnetic field at 2 mm and 50 mm above the ground plane. Compare the magnetic field radiated by the two groups of inductances. Conclude about this effect at circuit level.

Exercise 2: Radiated emission from an I/O bus
Four I/O are connected to terminal loads through PCB lines which form a bus. This exercise aims at studying the radiated emission in near and far field produced by the PCB lines.
The I/O are modeled by square generator, with the following characteristics:

- amplitude = 0 V to 2.5 V
- frequency = 10 MHz
- rise/fall time = 1 ns
- serial resistor = 10 Ω

The package influence is neglected. The power supply of the I/Os is considered ideal. All the I/Os are connected to 10 pF capacitive load through identical PCB line. The characteristic of the lines are:

- width = 0.25 mm
- thickness = 35 µm
- substrate height = 1.6 mm
- length = 5 cm

- separation between lines = 0.25 mm
- dielectric constant = 4.5

In a first time, PCB lines are designed on a one side PCB.

1. Build an electrical model valid over all the frequency range of signals flowing through the lines (use N parallel lines in the tool Interconnect Parameter). Select the option “Inductances used for Near field analysis”.

2. Simulate the radiated emission at 10 MHz from the PCB lines in near field (h = 1 mm) and far field (as the frequency is known, the limit between near and far field can be estimated). Do you think that this model is realistic?

3. Add a parallel line that connects the ground of the loads and the I/Os. Place this line at right to the fourth I/O. What is the effect on the radiated emission in near/far field? What is the best position for this new line?

4. Add a second line and find the optimum placement to reduce the most efficiently the radiated emission.

5. Remove the two added ground line and add a ground plane on the bottom side of the PCB. What is the effect on the radiated emission in near/far field?

7 Immunity Simulation

This section is dedicated to immunity simulation and prediction. Basic mechanisms of susceptibility to radiofrequency interferences have been presented in chapter 1. This chapter describes the simulation flow for susceptibility and concepts associated to susceptibility characterization. Different models of IC susceptibility are also proposed. As for IC emission modeling, using macromodels provides a good balance between efficiency and accuracy. Based on ICEM formalism (see chapter 5), a new proposal for IC susceptibility modeling called Integrated Circuit Immunity Modeling is on-going, as part of the general standard IEC 62433. Model examples proposed with IC-EMC follow the formalism provided by ICIM [7-1]. Moreover they put the emphasis on standard susceptibility measurement methods at IC level, defined by the standard IEC 62132 [7-2].

7.1 Characterization of the susceptibility of integrated circuits

Susceptibility to radio frequency interference is becoming a major concern for integrated circuits, with the multiplication of powerful parasitic sources such as mobile phones, high speed networks and wireless systems (Fig. 7-1). The trend for micro-miniaturization has two main consequences on integrated circuits (ICs) immunity. First, the constant supply voltage decrease reduces the noise margin of electrical signals and thus increases the IC susceptibility to RFI.

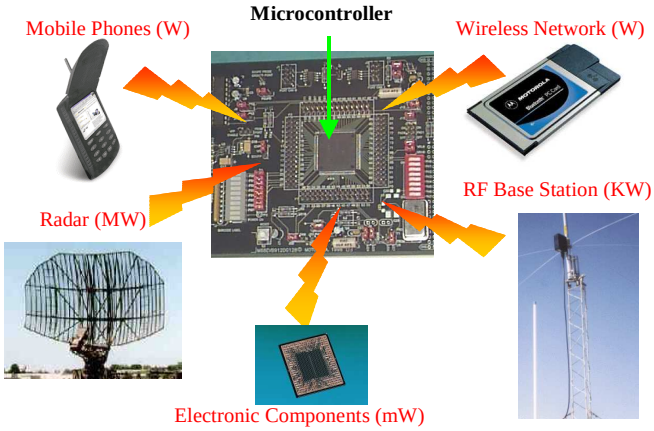
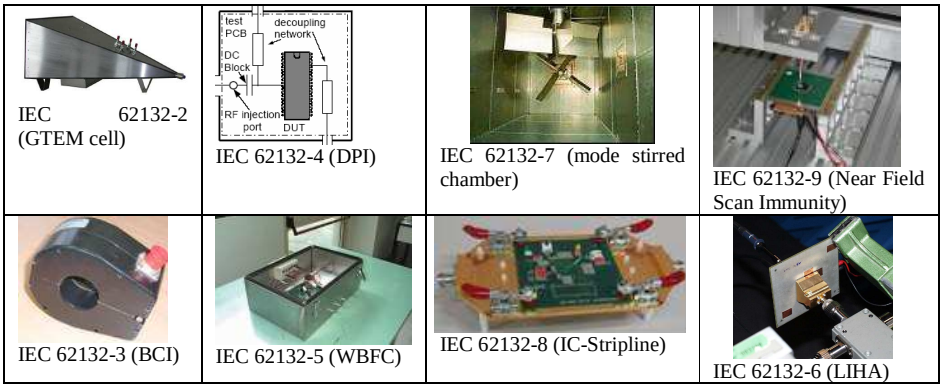


Figure 7-1: Parasitic radio-frequency sources which may disturb integrated circuits.

In order to ensure the robustness of ICs against electromagnetic interferences, ICs must pass susceptibility test measurement. The characterization of the susceptibility of an IC consists in injecting RF disturbances with either in conducted or radiated mode. The applied disturbances are either global or localized on one part of the device under test (DUT). The standard IEC 62132 defines methods to characterize susceptibility on the band 150 KHz – 1 GHz. Table 7-1 and 7-2 sums up the standard methods for characterization of immunity according to IEC 62132 and their status, while Table 7-3 describes the characteristics, the advantages and drawbacks of the most popular immunity characterization methods.



IEC 62132-2 (GTEM cell)

IEC 62132-4 (DPI)

IEC 62132-7 (mode stirred chamber)

IEC 62132-9 (Near Field Scan Immunity)

IEC 62132-3 (BCI)

IEC 62132-5 (WBFC)

IEC 62132-8 (IC-Stripline)

IEC 62132-6 (LIHA)

Table 7-1 : Measurement methods related to the IC emission standards IEC 62132 [7-3]

Standard	Description	Stage in 2009
IEC 62132-1	General and Definitions	International standard
IEC 62132-2	Transverse Electromagnetic, Cell (TEM), GigaHertz Transverse Electromagnetic Cell (GTEM)	International standard
IEC 62132-3	Bulk Current Injection (BCI)	Final draft international standard
IEC 62132-4	Direct Power Injection (DPI)	International standard
IEC 62132-5	Work Bench Faraday Cage (WBFC)	International standard
IEC 62132-6	Local Horn Injection Antenna (LIHA)	New proposal
IEC 62132-7	Mode stirred chamber	New proposal
IEC 62132-8	Micro strip-line	New Proposal
IEC 62132-9	Near field scan immunity (NFSI)	New proposal

Table 7-2 : Roadmap for standard IEC 62132 - Measurement of IC susceptibility up to 1GHz [7-3]

Name of the method	Nature of the coupling	Frequency band	Advantages	Drawbacks
Direct Power Injection (DPI)	Conducted	100KHz to 1GHz	Low power needed Low cost	Parasitics of the injection capacitance
Bulk Coupling Injection (BCI)	Conducted	1MHz to 400MHz	Adapted for cable injection	Need high power
TEM/GTEM	Radiated	1MHz to 1GHz / 1MHz to 18GHz	50 Ω adapted injection path	Low coupling with the DUT
Anechoic chamber	Radiated	> 30MHz	Isolated environment	Need much space Expensive

Table 7-3 : Characteristics of the most popular measurement methods to characterize immunity of ICs [7-2]

Figure 7-2 describes the general experimental set-up for the susceptibility measurement of a circuit. The set-up includes three parts:

- the generator of Radio Frequency Interferences (RFI), dedicated to the generation of a disturbance with a given waveform (sinus, pulse, burst), frequency (150 KHz to 1 GHz for IEC 62132 standard), and amplitude (typically given in term of power). Maximum levels of power are recommended for each method, e.g. 25 or 30 dBm for DPI method. Disturbance generation is usually composed of a RF signal synthesizer followed a power amplifier.

- an injection path which transfer the disturbance to the circuit under test. It is recommended to match the injection path to avoid multiple reflections. Most of the time, special devices are inserted in the coupling path as directional coupler to measure the actual forward power and

attenuator to reduce infinite VSWR issues which can degrade amplifier outputs. The coupling of the disturbance to the circuit depends on the method. It can be radiated or conducted.

- the detection of failure of the circuit which determines if the device under test (DUT) works correctly or fails. The notion of failure depends on the definition of one or several failure criteria related to the nature of the circuit, the final application and its constraints. Circuits for mass market and circuits for critical embedded systems have not the same tolerance level to failures so that failure criteria for these two types of application are not the same. The usual susceptibility criteria are the noise level on power supply or output signal, the appearance of erroneous state on a digital signal, a too large jitter on a clock, an accidental reset, an over current. Oscilloscopes with pattern generation are often used to detect failures as overrated noise or erroneous logical state.

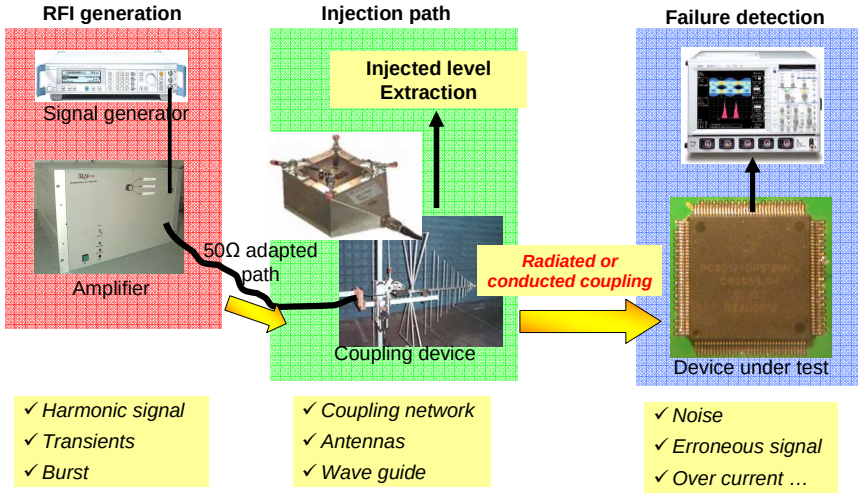


Figure 7-2: Generic setup for IC immunity characterization

7.2 Flow for immunity simulation

Most of the time, EMC of IC models are validated by measurements done on a circuit mounted on specific EMC board and in a minimalist configuration. Once the model of the circuit has been validated, it can be included in a larger model to simulate the immunity of a complete electronic systems, which includes several circuits, PCB tracks and planes, connectors, cables…). One key objective of IC-EMC is to help the user to build EMC of IC models and validate them through comparisons with measurements.
The general flow used to achieve a comparison between measurement and simulation of susceptibility to a harmonic RFI is described in figure 7-3. On one side, the immunity measurement is performed using the standardized test bench (DPI, BCI, Near-field, etc.). The result is susceptibility threshold curves which consists in the power in dB-milliwatt (dBm) required to induce a failure versus the frequency of the RFI. To build the model of the aggression of the DUT, we rely on package information given by IBIS, the core model given by ICEM, and the injection path model including the RFI generator, directional coupler, attenuators, coupling devices and all the cables and PCB tracks.

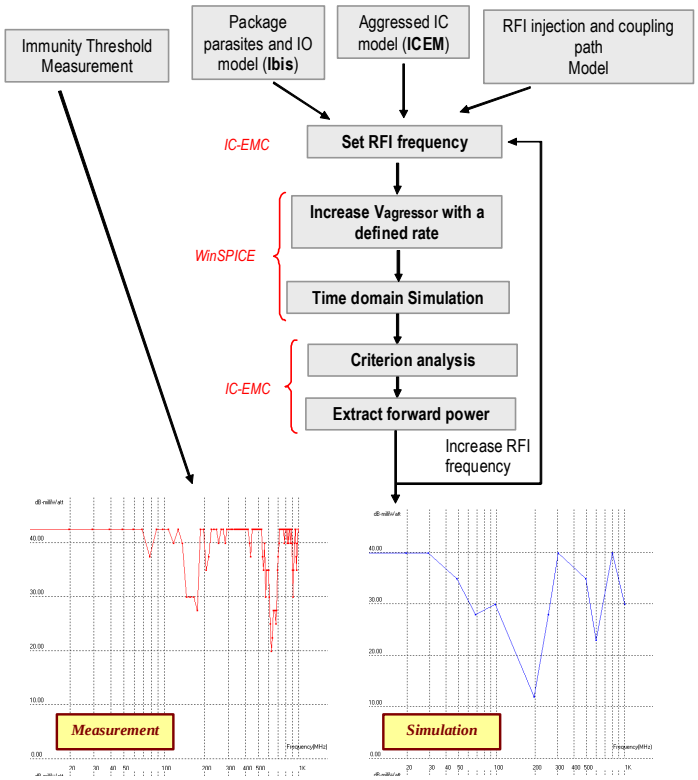


Figure 7-3 : Methodology to compare measured and simulated immunity of ICs to harmonic RFI

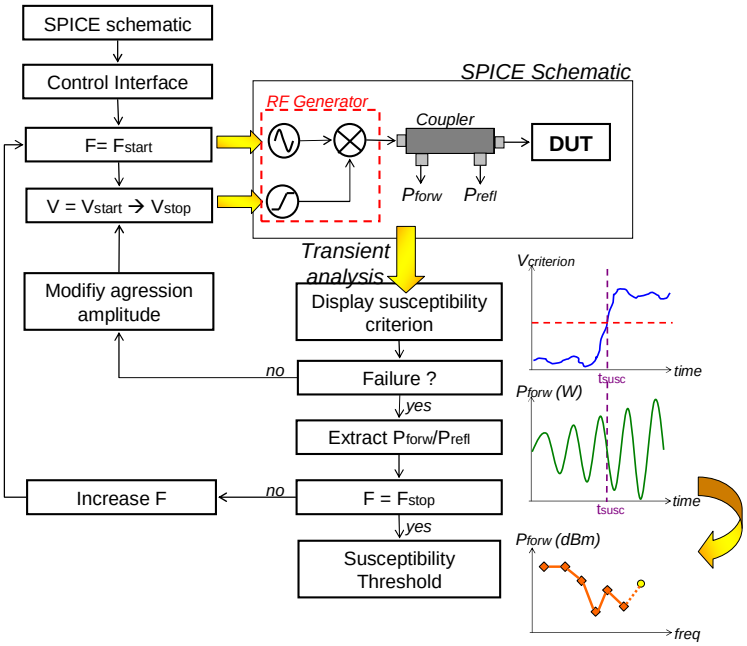


Figure 7-4 : Simulation flow used to extract the susceptibility threshold of a circuit

To determine the immunity level of a component, a susceptibility criterion has to be defined which applied both on measurement and simulation. The simulation of susceptibility to a harmonic disturbance is based on an iterative process with a varying frequency, as described in figure 7-4. For each frequency point, the

amplitude of the RFI is increased until one of the susceptibility criterions reaches a defined limit. For example, a common susceptibility criterion based on the level of noise is reached when the fluctuation of a voltage exceeds +/- 20 % of the nominal power supply voltage, as illustrated in figure 7-5.

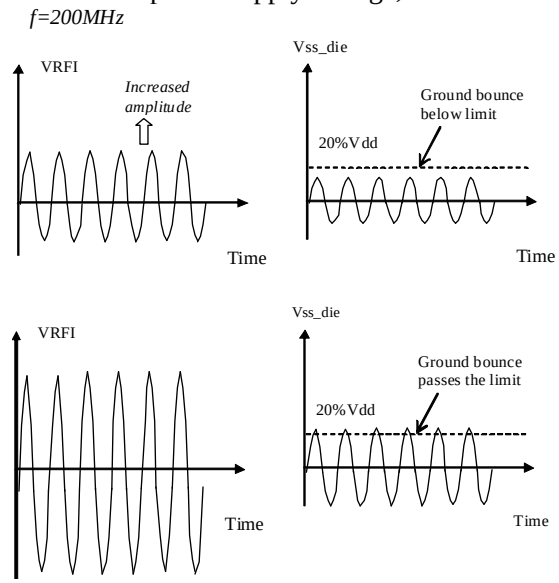


Figure 7-5 : The RFI amplitude is increased until the ground bounce amplitude goes over a susceptibility threshold (20% supply voltage)

7.3 ICIM model

Similarly to IC emission modeling, a standard model for IC immunity prediction is currently on development. Integrated Circuit Immunity Model (ICIM) is a new proposal from TC47 group of IEC known as IEC 62433-4 [7-1]. This model is based on ICEM architecture and formalism, but it aims at deriving a macro-model to simulate of the immunity level of an analog or digital IC to conducted or radiated disturbances. Compared to emission model, immunity model is more difficult to establish because it must describe the behavior of the circuits to RF disturbances and keep a sufficient level of simplicity and confidentiality [7-4]. As ICEM, ICIM does not impose a description language, but format like SPICE, VHDL-AMS or Verilog are particularly adapted.
Like ICEM, ICIM structure is based on a set of basic components which models functional blocks of a circuit (e.g. a digital core, an I/O, an analog to digital converter…). Two types of basic components are proposed in ICIM formalism, as described in figure 7-6:

- Passive Distribution Network (PDN) which is similar to the PDN in ICEM. The PDN describes the impedance network across one or several terminal, e.g. the power distribution network of a digital core. Physically, the PDN includes passive elements as package lead, bonding and on-chip interconnections. The PDN has a major influence on circuit susceptibility as it acts on the propagation, filtering and distortion of RFI.

- Immunity Behavior (IB): this component replaces the Internal Activity block in ICEM. It describes how the circuit will react to a disturbance. While PDN can be modeled entirely with passive elements, IB component can have a non linear behavior and must embed non linear or active components. The IB produces a behavioral output which allows the detection of a failure for a given susceptibility criterion.

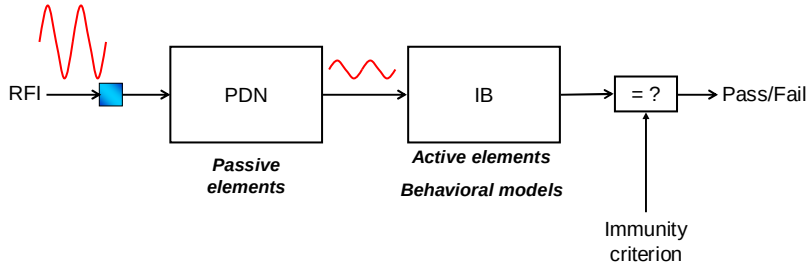


Figure 7-6 : Structure of ICIM [7-1]

As ICEM, ICIM can be included in a larger model which contain the models of RFI injection systems, the PCB on which the component is mounted and all the system. The ICIM standard does not recommend a specific description methodology for the IB component, but it proposes different possibilities, such as an equivalent electrical model, a mathematical representation or a simple criterion.

7.4 Power measurements- Directional coupler model

Susceptibility measurements make an extensive use of power units, especially dBm.

7.4.1 Power units

The measurement of power is an important issue during IC susceptibility tests. Typically, immunity levels are given in terms of forward, reflected and/or transmitted power to detect the failure of the device under test (DUT). However electrical simulators like SPICE work with voltages and currents. This creates some difficulties to compared measured and simulated power. The typical unit for power measurement is the dB milliwatt (dBm). The link between dBm and linear Watt is recalled in equ. 7-1.

$$P(dBm) = 10 \times \log(P(W)) + 30 \qquad \textit{Equ. 7-1}$$

7.4.2 Directional Coupler Theory

A directional coupler is a passive device which enables the separation and the measurement of both the forward and reflected waves within the coupler. As explained in the chapter Basic Concepts, both waves result from the mismatch between the load impedance and the characteristic impedance of the line. A part of the forward wave is effectively transmitted to the load whereas the other part of the original wave is reflected and comes back to the source through the transmission line. A directional coupler has one main input usually connected to the power amplifier and one main output connected to the device under test.
The characteristic impedance of the coupler Zc is 50 Ω. The delay line between the input and output port has a length of 40 cm, embedded in a dielectric with epsr=2.2. The corresponding delay is 2 ns. The two other terminations capture a fraction of the forward and reflected wave for power measurement purpose. The attenuation between the power measured in these ports and the real power through the coupler is 20 dB. Figure 7-7 shows a picture of a directional coupler (Reference HP 778D, with a bandwidth from 100 MHz to 2 GHz) and a description of the ports.

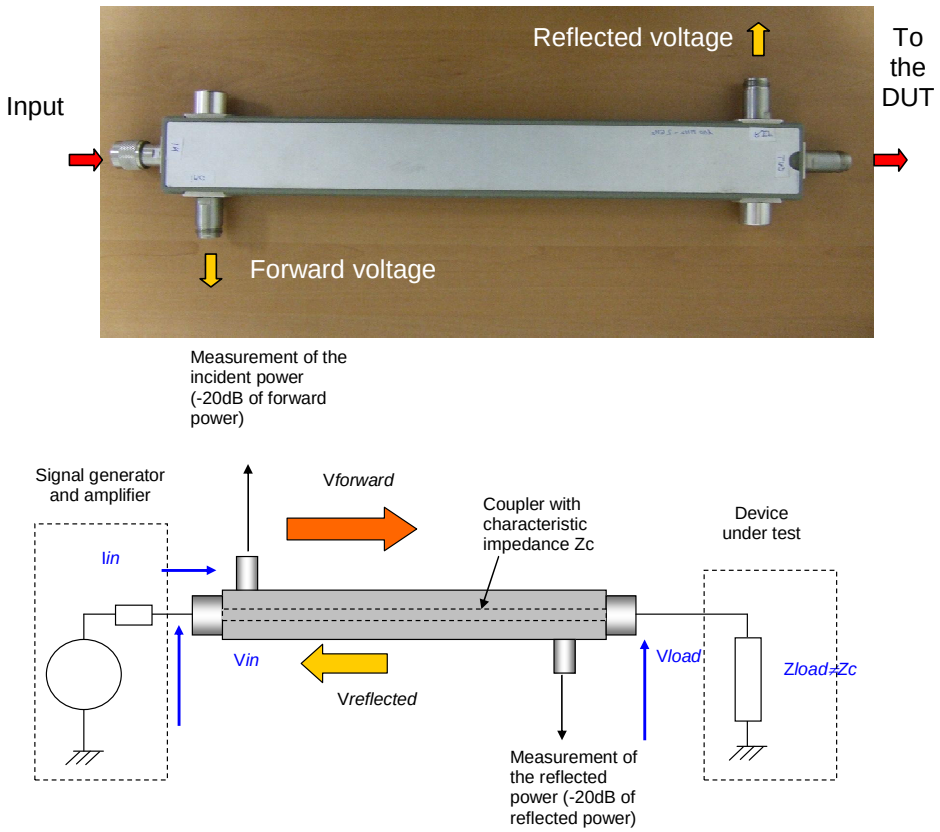


Figure 7-7 : details on the coupler used for measuring forward and reflected power

Figure 7-8 presents the main properties of the coupler HP 778D:

- Input reflection. As it induces insertion losses, input reflections should be as small as possible.
- Transmission, between the input to the output connected to the device under test.
- Coupling, which characterize the ratio between the power measured on the terminal forward power and the power of the forward power.
- Isolation characterizes the coupling between the forward power and the terminal used to measure the reflected power. The coefficient that characterizes the isolation should be as small as possible.

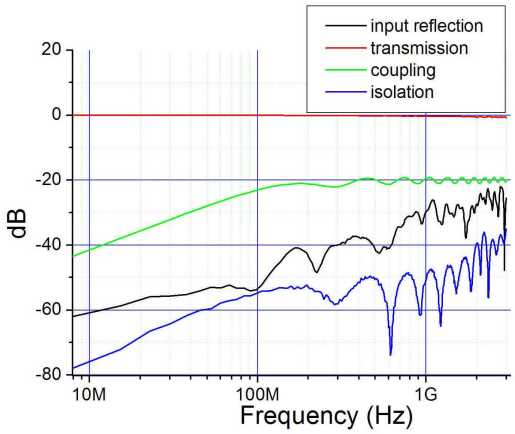


Figure 7-8 : Characteristics of the coupler HP 778D

The forward and reflected voltages can be expressed as complex numbers by Equations 7-2 and 7-3. It is related characteristic impedance and the length of the line that they cross and with the termination impedance. In other terms, it depends on the mismatch ratio. These two values can be computed with the following formulas:

$$V_{forward} = \frac{V_{in} + Z_c \times I_{in}}{2} \quad \textit{Equ. 7-2}$$

$$V_{reflected} = \frac{V_{in} - Z_c \times I_{in}}{2} \quad \textit{Equ. 7-3}$$

Where
Vforward is the forward voltage (V)
Vreflected is the reflected voltage (V)
Vin is the complex voltage at the input of the coupler (V)
Iin is complex current at the input of the coupler (A)
Zc is the characteristic impedance of the coupler (Ohm)

$$P_{forward} = 10 \times \log\left[\frac{1}{Z_c} \times \left(\left(\frac{real(V_{in}) + Z_c \times real(I_{in})}{2}\right)^2 + \left(\frac{imag(V_{in}) + Z_c \times imag(I_{in})}{2}\right)^2\right)\right] + 30 \quad \textit{Equ. 7-4}$$

$$P_{reflected} = 10 \times \log\left[\frac{1}{Z_c} \times \left(\left(\frac{real(V_{in}) - Z_c \times real(I_{in})}{2}\right)^2 + \left(\frac{imag(V_{in}) - Z_c \times imag(I_{in})}{2}\right)^2\right)\right] + 30 \quad \textit{Equ. 7-5}$$

Where
Pforward is the forward power in dB-milliwatt (dBm)
Preflected is the forward power in dB-milliwatt (dBm)

Considering that the coupler impedance Zc is 50 Ω, the forward and reflected power can be expressed by Equ. 7-4 and 7-5. The power transmitted to the load can be derived from these formulations as follows:

$$P_{transmitted}(W) = P_{forw} - P_{refl} \quad Equ.\ 7\text{-}6$$

7.4.3 Directional Coupler Implementation

A model of an ideal directional coupler is proposed in the symbol palette of IC-EMC, as described in figure 7-9. The coupler is characterized by characteristic impedance and a propagation delay as any transmission line. If selected, forward and reflected power can be computed. Immunity simulation requires the presence of a coupler in the schematic to extract the forward power.

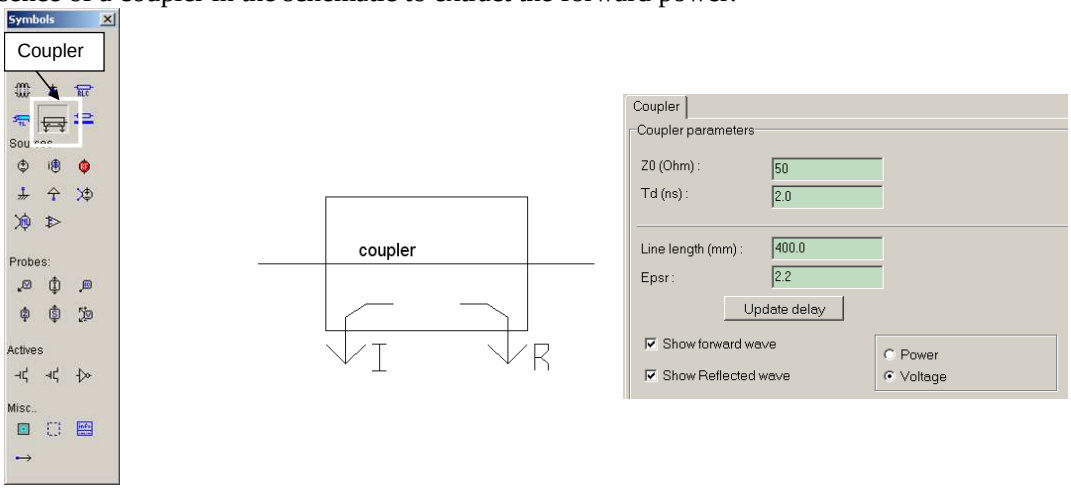


Figure 7-9 : Coupler symbol and properties

7.5 A simple coupler simulation

7.5.1 Matched load simulation

The first validation case is an ideal 50 Ω resistive load connected to a voltage generator by a through the coupler. The schematic diagram of Fig. 7-10 is used to simulate the forward and reflected power in the frequency range 1 MHz-3 GHz. Note that the AC simulation is configured with the text ".AC DEC 100 10MEG 3G".

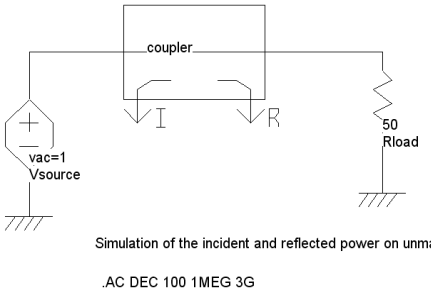


Figure 7-10 : Simulation of forward and reflected powers to a 50 Ω load (immunity/coupler/coupler_power.SCH)

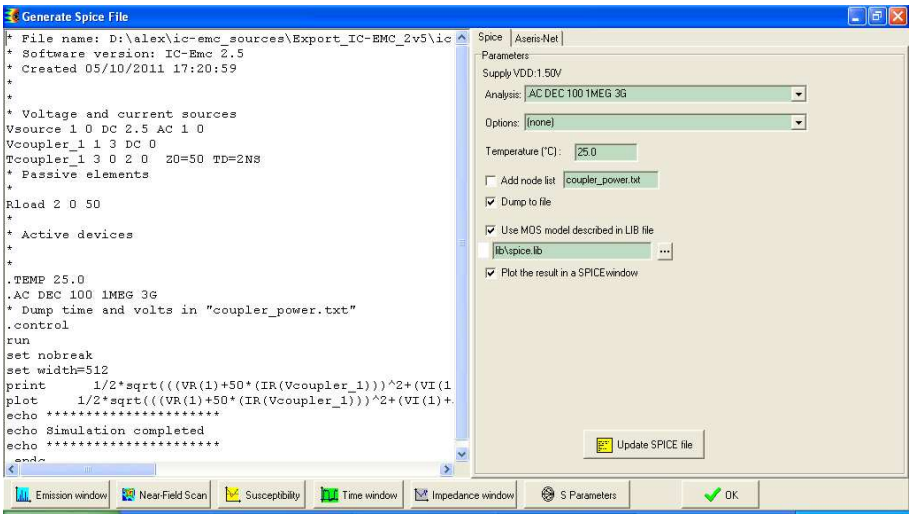


Figure 7-11 : SPICE netlist for the coupler example (immunity/coupler/coupler_power.SCH)

The SPICE netlist corresponding to the coupler simulation is shown in Fig. 7-11. Notice the description for the forward and reflected power according to equations 7-4 and 7-5. The result given by WinSPICE is in Watt, but the post-processing in IC-EMC converts the Watt into dBm. Click on "EMC/Susceptibility dBm vs. frequency" or on the icon  in order to display the simulated forward and reflected power in the susceptibility interface, as shown on figure 7-12.

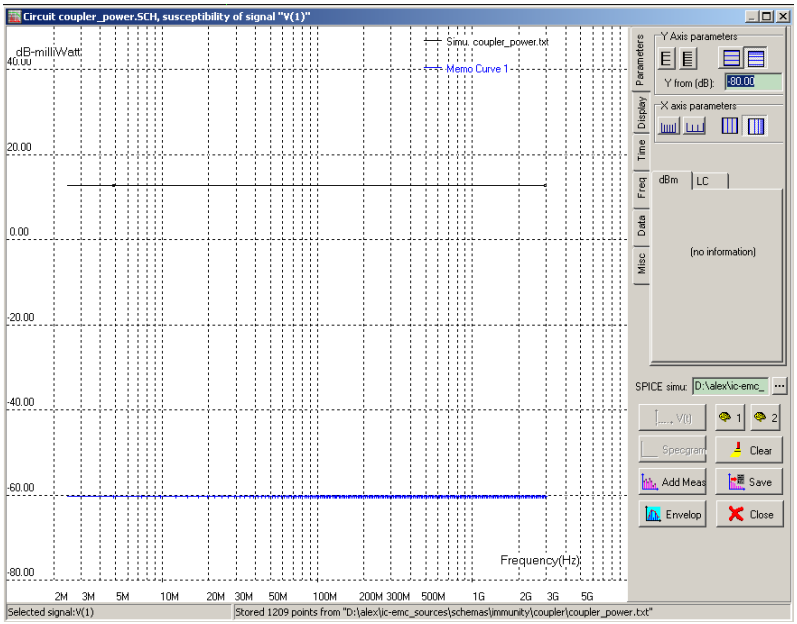


Figure 7-12 : Forward and reflected power in dBm (immunity/coupler/coupler_power.SCH)

The situation corresponds to a 50-Ω transmission line (the coupler) terminated by a 50 Ω load, resulting to a null reflected power and a maximum forward power. A default value of -60.0 dBm is assigned by default when the value in W is lower that 1nW, as shown in fig. 7-12. As the voltage source amplitude is 1 V and the load is 50 Ω, the forward power may be computed by Equ. 7-7, which is equal to the simulate result:

$$P_{forward} = 10\log(\frac{V_{in}^{\ 2}}{R_{load}}) + 30 = 10\log(\frac{1}{50}) + 30 \approx 13dBm \qquad \textit{Equ. 7-7}$$

7.5.2 Unmatched load simulation

If the value of the load resistor *Rload* becomes significantly different from the coupler characteristic impedance *Z0*=50 Ω, a mismatch is created and the reflected power is no more zero. Hence resonances and anti-resonances appear in the coupler. In this example (*Rload*=150 Ω), resonances appear every multiples of a value close from 120 MHz. The amplitude of the resonances depends on the mismatch.

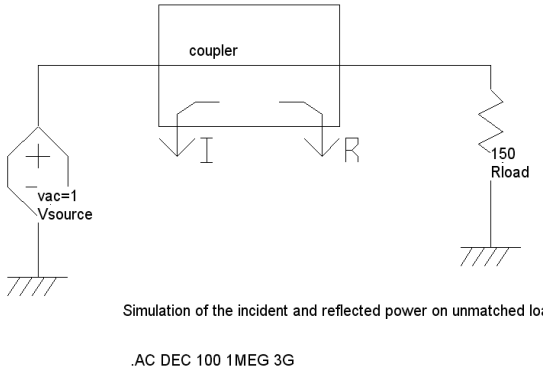


Figure 7-13 : Simulation of forward and reflected powers to a 150 Ω load (immunity/coupler/coupler_power_150ohm.SCH)

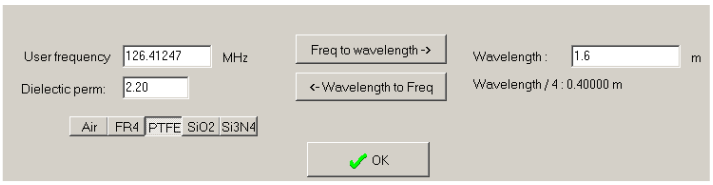
7.5.3 Link between delay and resonance

The coupler is equivalent to a transmission line. When one-fourth of the input wavelength ($\lambda/4$) matches the coupler length l=40 cm, a resonance effect is observed in Fig. 7-14. The relation between the resonant frequency, the wavelength, coupler length and the dielectric permittivity is given by Equ. 7-8.

$$f = \frac{c}{\lambda\sqrt{\varepsilon_r}} = \frac{c}{4l\sqrt{\varepsilon_r}} \qquad \textit{Equ. 7-8}$$

Where:
λ = wavelength (m)
l = coupler length (m)
c = speed light (3 x 10^8 m/s)
f = resonant frequency at $\lambda/4$ (Hz)
ε_r=dielectric permittivity

We can compute the first resonant frequency using the tool "Tools → Freq/Wavelength converter". The wavelength is equal to 4 times the coupler length (1.6 m), which gives 126 MHz. At $\lambda/2$, the wavelength is equal to 2 times the coupler length (0.8 m) which gives 252 MHz which corresponds to a local minimum of the power. At $3\lambda/4$, the wavelength is equal to 4/3 times the coupler length (0.53 m), which leads to 380 MHz.



7.5.4 Reflection coefficient

In low frequency, the values of the forward and reflected powers tend to 9.5 dBm (8.9 mW) and 3.5 dBm (2.24mW) respectively. The command "Tools → dB/Linear Unit Converter" may be used to make this conversion. The reflection coefficient Γ may be computed by Equ. 7-9 or 7-10. Equations shows the exact correlations between the two methods to compute the reflection coefficient.

$$|\Gamma| = \left|\frac{V_{refl}}{V_{forw}}\right| = \sqrt{\frac{P_{refl}}{P_{forw}}} = \sqrt{\frac{2.24}{8.9}} = 0.5 \quad \textit{Equ. 7-9}$$

$$|\Gamma| = \left|\frac{Z_{load} - Z_c}{Z_{load} + Z_c}\right| = \left|\frac{150 - 50}{150 + 50}\right| = 0.5 \quad \textit{Equ. 7-10}$$

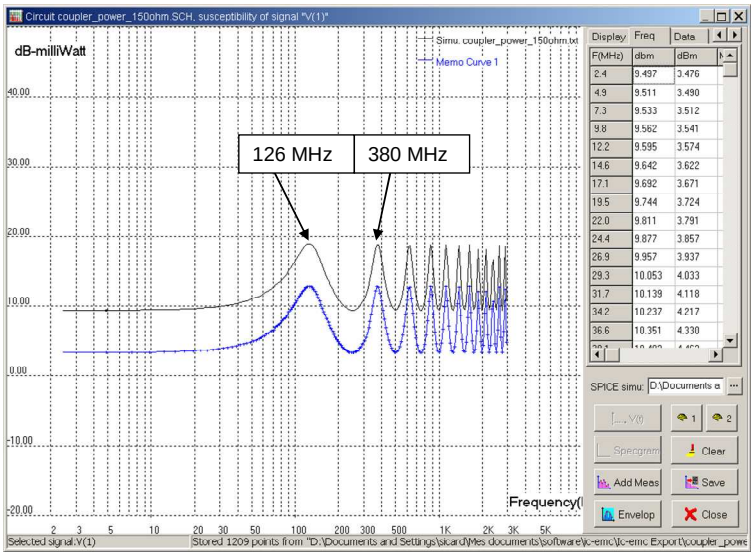


Figure 7-14 : Simulation of forward and reflected powers to a 150 Ω load (coupler_power.sch)

7.5.5 Transmitted power

The power transmitted to the 150 Ω load is the simple subtraction between the forward and reflected power (Eq. 7-11). The transmitted power is about 6.7 mW.

$$P_{transmitted}(W) = P_{forw} - P_{refl} = 8.9 - 2.24mW = 6.66mW \quad \textit{Equ. 7-11}$$

Most susceptibility measurements are based on forward power. Measuring both the forward and the

reflected power and calculating the reflection coefficient can however be helpful.

7.6 Direct Power Injection

The Direct Power Injection (DPI) [7-5] is a common method used to characterize the conducted susceptibility of ICs. Most of the susceptibility measurement examples presented in this guide are based on this method. We rely on DPI to present the susceptibility simulation flow and the different element used in the schematic.

7.6.1 The DPI standard

The DPI method consists in applying a conducted RF disturbance to any I/O pins of an integrated circuit. The RF disturbance is usually superimposed to a low frequency signal as a digital signal or a power supply, through a DC block capacitor. Most of the time, a decoupling network is added to prevent RF disturbances flowing into DC supply or digital signal source. Figure 7-15 describes the DPI set-up. The DUT is usually mounted on a specific test board. RF disturbances are generated by an RF generator followed by a power amplifier. The use of a directional coupler is recommended to control during the test the level of forward power.
The coupling capacitance and the decoupling network are set in order to optimize the transfer of RF disturbances to the tested pin, within the frequency range of the test. As most of the susceptibility tests given by the standard IEC 62132, the DPI standard is given for the frequency range 150 KHz – 1 GHz.

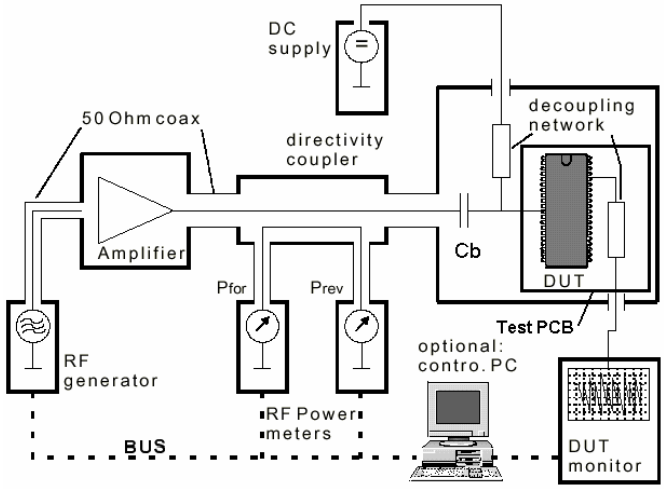


Figure 7-15: Set-up for immunity testing using DPI method [7-4]

Remark: an attenuator is usually inserted in the injection path, just after the power amplifier. This device provides a constant attenuation over a wide frequency range and matched input and output. Even if it reduces the amount of forward power of the RF disturbance, it also decreases the amount of reflected power. Therefore, it prevents from a too large voltage standing wave ratio (VSWR) at the power amplifier output which could reach very unacceptable high values when the connected load is unmatched. A too large VSWR can lead to a degradation of the output stage of the power amplifier. The ideal case would consist in a load nearly equal to the characteristic impedance of the cable and injector impedance over the whole frequency range. Whatever the value of load, the presence of the attenuator reduces the VSWR.

7.6.2 Radio Frequency Interference (RFI) Source in IC-EMC

IC-EMC proposes a specific source called *Radio-Frequency Interference* (RFI) source to model a source of harmonic disturbances, similar to the signal generator and the power amplifier of the

susceptibility test bench. In continuous wave (CW) immunity tests, the forward power which induces a disturbance is determined for each frequency using a step-by-step increase of the forward power as described in figure 7-4. This principle is reused in simulation. The disturbance level generated by the RFI source at a given frequency is increased linearly between two voltage bounds for all the simulation duration. After the simulation, a post-processing tool detects if a failure appear and extract the forward power amount when the failure appears.

Figure 7-16 presents a simple schematic to present the RFI source. The RFI source is connected to a 50 Ω load. The RFI source is a sinusoidal wave with programmable voltage increase from V0 to V1 for a given duration T0. The RFI source also includes a default 50-Ohm serial resistance. The source parameters are listed in Fig. 7-17.

The simulation must be a transient simulation. Note the presence of the command line ".fail 0.25" that defines a failure criterion. If the voltage across the resistor Rload exceeds 0.25 V, a failure is detected.

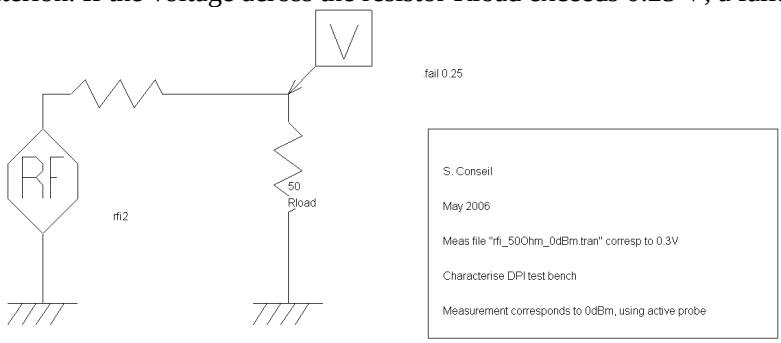
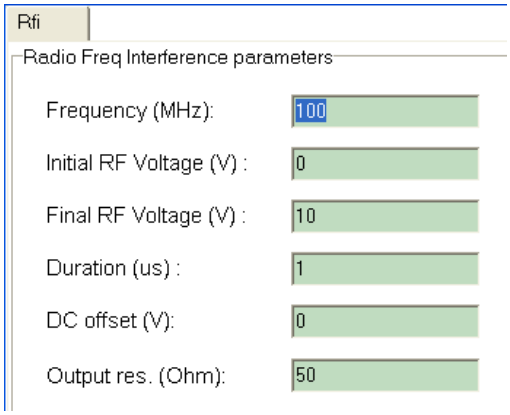
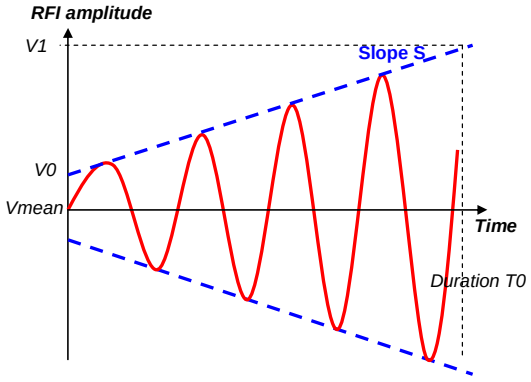


Figure 7-16 : The RFI source example (immunity/rfi/rfi_50ohm.sch)





Parameter	Name	Default Value
Frequency	FREQ	100 MHz
Initial Voltage	V0	1 V
Final voltage	V1	10 V
Duration	T0	1 µs
DC offset	Vmean	0 V
Output resistor	R_RFI	50 Ω

Figure 7-17 : RFI source parameters

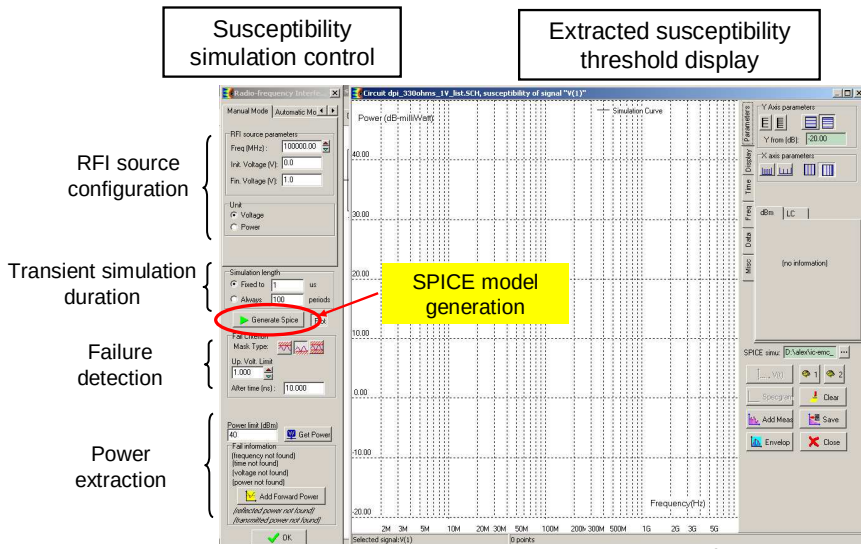


Figure 7-18 : Susceptibility simulation interface

The SPICE netlist should not be generated directly from the main window of IC-EMC, but from the post-processing tool dedicated to susceptibility simulation. Click "EMC → Susceptibility dBm vs. Frequency" or on the icon . The window described in figure 7-18 appears. The susceptibility simulation tool has two parts: a control of the simulation and the display of the extracted susceptibility threshold. RFI source parameters and transient simulation length are configured from this tool.
The susceptibility tool offers three simulation modes, which depends on the sweeping method of the RFI frequency (we assume harmonic disturbances and remember that we want o extract the required forward power level for each harmonic frequency, as explained in figure 7-4):

- Manual simulation mode: the user configures a transient simulation for only one RFI frequency. The frequency sweeping is performed manually by the user. A SPICE simulation is launched for each RFI frequency and the user has to extract the forward power after each simulation.

- Automatic simulation mode (default mode): the user configures N transient simulations for N RFI frequency points. The frequency sweeping is configured by the user and automatically done by the SPICE simulator. At the end of SPICE transient simulation, IC-EMC extracts the forward power level for the N frequency points and plots the susceptibility level. The frequency sweeping can be linear or logarithmic. The RFI source amplitude and simulation duration parameters are defined by the user in the Susceptibility tool interface, and remain the same during all the simulation (i.e. for the N frequency points).

- List simulation mode: the same principle than the automatic simulation mode (the frequency sweeping is configured by the user and automatically done by the SPICE simulator), except in the configuration of RFI source amplitude and simulation duration parameters. They are predefined individually for each of the N RFI frequency points in a text file (see part 1.8 for more information about the file format). This mode is interesting for simulation which cover large frequency ranges (several decades) and when the sensitivity of a circuit to RFI varies considerably with the frequency.

After configuring the RFI source and the transient simulation (set the simulation duration to 1 µs), click on the button "Generate SPICE" to launch the transient simulation. Voltage across the resistor Rload and

internal voltage of the RFI source are computed for 0.5 µs. At the end of the simulation, return to the susceptibility simulation tool. Click on the button "Get Power" to extract the power delivered by the generator. On the display window, the voltage across the resistor Rload is plotted. A straight line indicates the voltage associated to the failure criterion. As the 50 Ω is in series with the load, the resulting voltage at the load termination rises from 0.0 V to 1 V, which is half of the generated voltage.
When no coupler is present in the schematic, the forward and reflected power can not be extracted. Instead the maximum available power from the source P_{Avmax} is computed using equation 7-12.

$$P_{AV\,\max} = \frac{V^2}{4 \times Z_C} \qquad \textit{Equ. 7-12}$$

When the output voltage passes the voltage threshold, the power delivered by the source is equal to 1.26 mW or 1 dBm, which fits with the theoretical value. As the load is matched on the output impedance of the RFI, The power delivered to the load is equal to the maximum available power of the source. When the failure is detected, the voltage across the load is equal to 0.25 V, so that the power delivered to the load is equal to 1.25 mW.

7.6.3 Direct Power Injection on a 330 Ω load

This section concerns a simple case-study using the Direct Power Injection (DPI) measurement on a resistive load of 330Ω. DPI measurements are compared to simulation in order to validate the immunity simulation module.

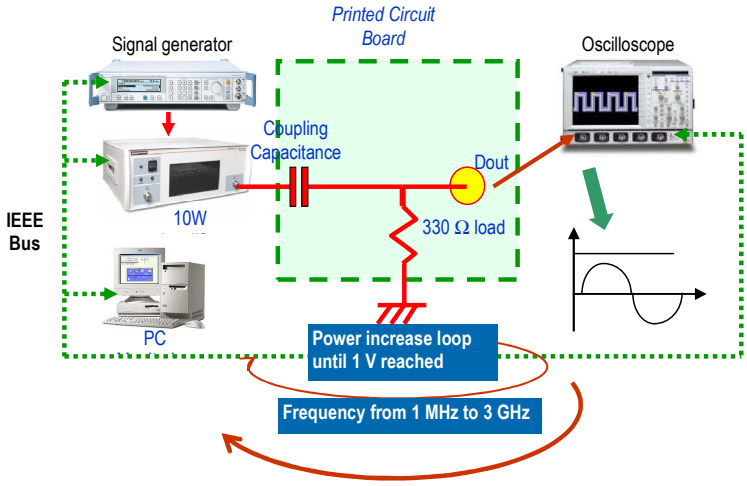


Figure 7-19 : injection on a 330 Ω load through a 1nF capacitor

Figure 7-19 shows the principle of the experimental test set-up. A first loop consists in increasing the power until the 1 V voltage threshold is reached. The second loop concerns the frequency. Typically, 10 points per decade are measured, from 1 MHz to 3 GHz. The printed circuit board used for this experiment is shown in Fig. 7-20. To minimize high frequency parasitic effects, tracks are routed the shortest possible. The two sides of the printed circuit board are described, with the two surface-mounted components and the SMA connectors.

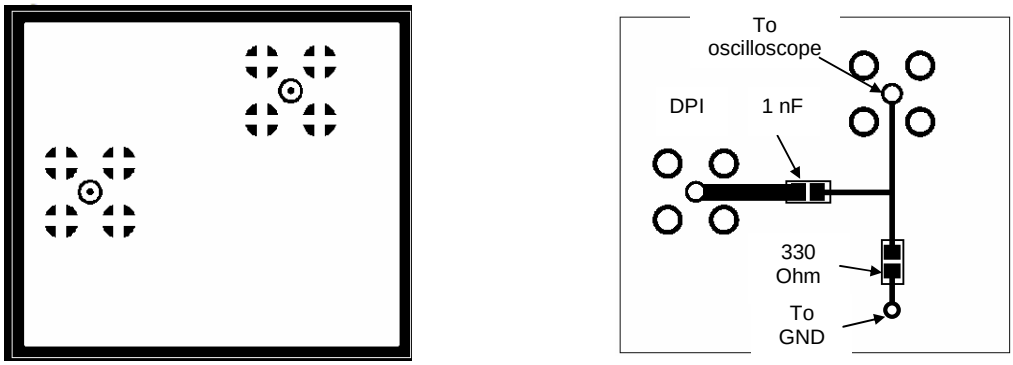


Figure 7-20: DPI board layout

A signal generator creates a continuous wave with programmable frequency (here 10 MHz to 500 MHz). A signal amplifier produces the forward wave which is injected through a 1-nF capacitor to a resistive load of 330Ω. The coupler situated between the amplifier and the test board enables the measurement of both the forward power and reflected power, through a 2-channel power meter. The power meter gives the root-mean-square (RMS) value of the power.

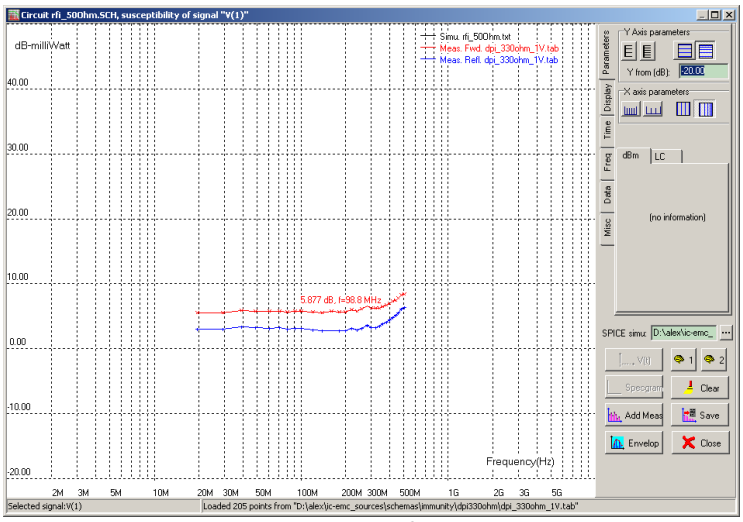


Figure 7-21: Measurement result of DPI injection with an active probe (immunity\dpi330ohm\dpi_330ohm_1V.tab)

To measure the voltage across the 330 Ω resistance, we use a digital oscilloscope connected to the SMA connector via an active probe. The sample frequency of the oscilloscope is equal to 500 MHz. The susceptibility criterion is the resistance voltage exceeding 1V, measured by an active probe. Figure 7-21 presents the measured forward and reflected power. To display the result, click “Add Measure” and select the file “immunity\dpi330ohm\dpi_330ohm_1V.tab”.

7.6.4 Manual simulation of a DPI on a 330 Ω load

In this paragraph, a simple DPI model is built to predict the susceptibility threshold on the 330 Ω load. The schematic diagram consists, from left to right of fig. 7-22, of a RFI generator, a coupler, a 1 nF capacitor (Cdpi), a 330 Ω load, and a 1-MΩ resistor in parallel with a 1.6 pF capacitor which account for

the active probe model. The text ".fail 1.0V" indicates that the threshold voltage is set to 1.0V.
The susceptibility simulation consists in finding the forward power starting which the voltage across the 330 Ω load exceeds 1 V. The simulation is manually controlled from the RFI control interface shown in Fig. 7-23. This window is opened by the command "EMC→Susceptibility (dBm) vs frequency" or by "View → RFI Control". The user's interface features a simple control of the RFI parameters, the generation of the WinSPICE netlist and the extraction of the power level according to a given susceptibility threshold. The interface is in automatic mode by default. Select the Manual Mode tab.

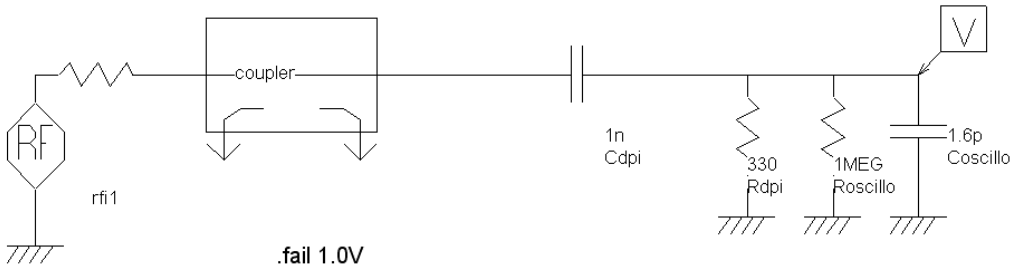


Figure 7-22: Model of a DPI injection on a 330 Ω load (immunity\dpi330ohm\dpi_330_1V.sch)

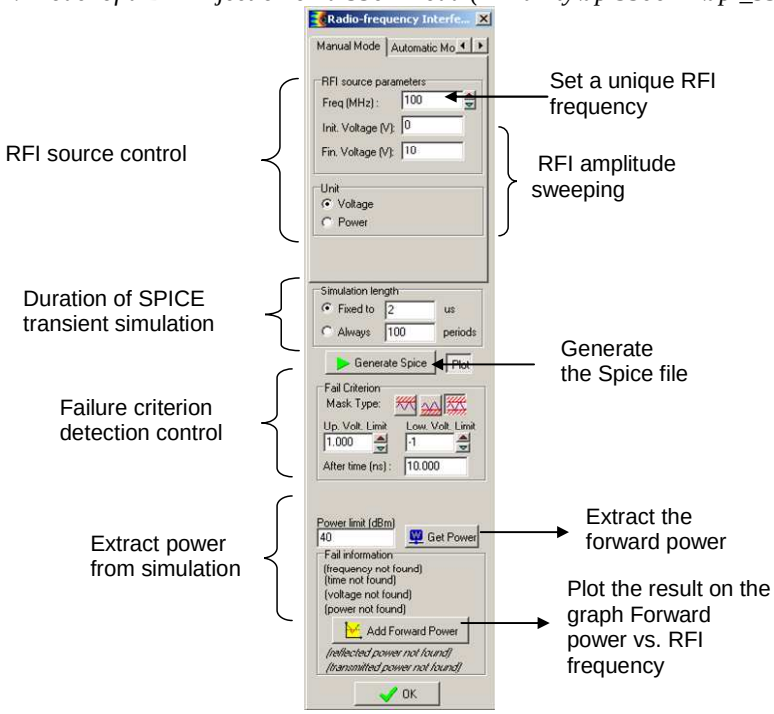


Figure 7-23: RFI control window in manual mode

To simulate the circuit and extract the forward and reflected power, proceed as detailed below in table 7-4.

Step	Details	Comments
Set the RFI source parameters	The default parameters for the RFI source are a 100-MHz frequency, the unit is "Voltage", a voltage from 0 to 10 V and a duration of 1 µs.	The frequency may be changed step-by-step
Set the transient simulation duration	The default simulation duration is equal to 1 µs. Enter '2' in the filed "Fixed To (µs)". The simulation duration can also be defined in terms of RFI period (e.g. if	The accuracy of the susceptibility simulation increases with the simulation duration. For a given amplitude sweeping, defining the

	the RFI frequency = 100 MHz, 100 periods sets a simulation duration equal to 1 µs.	simulation duration in term of RFI period ensures a constant accuracy whatever the frequency.
Set the susceptibility criterion	In the section “Fail Criterion”, select the voltage mask type to detect the susceptibility criterion, and enter the values ‘1’ and ‘-1’ in the field “Up Volt. Limit” and “Low Volt. Limit”.	The value may be predefined using a label with the syntax “.fail 1.0”.
Simulate	Click “Generate Spice”. Launch WinSPICE and open the file *rfi_dpi_330_1V.cir*.	
Extract the power	Click “Get Power” to extract the forward, reflected and transmitted powers.	RMS values of powers are given. The susceptibility threshold is given in term of forward power.
Extract the power	Click “Add Forward Power” to add the extracted value in the graph “dBm vs. frequency”.	

Table 7-4 : Steps to extract susceptibility threshold in simulation

Figure 7-24 shows the time-domain waveform and the extraction of the time at which the susceptibility threshold of 1 V is attained. At 100 MHz, the corresponding forward power is 5.7 dBm and the reflected power is 2.4 dBm. These values are close to the measured powers which are respectively equal to 5.9 and 3.2 dBm. Change the frequency and go through steps 3 to 5. Repeat the same process for different RFI frequency and extract the forward power for each RFI frequency. Figure 7-25 shows the susceptibility simulation results with comparison to the measured forward power. Click “Save” to store the simulation results in a data file.

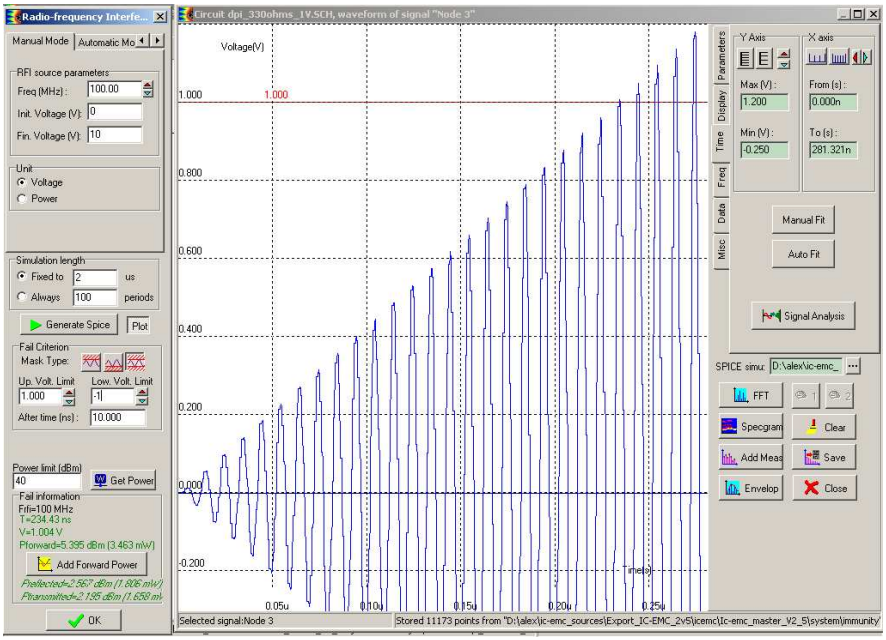


Figure 7-24: Extraction of the susceptibility threshold (immunity\dpi330ohm\dpi_330_1V.sch)

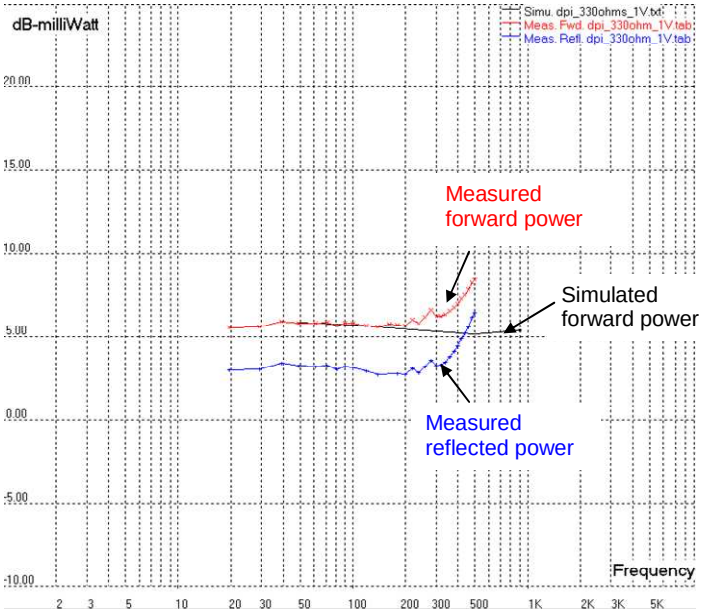


Figure 7-25: Comparison between measurement and simulation of DPI on a 330 Ω load (immunity \ dpi_330_1V.sch)

The simulated susceptibility threshold fits on the measurement up to 200 MHz, where the required forward power is almost constant. Above 200 MHz, the measured forward power increases, but this trend is not reproduced in simulation. The discrepancies with the measurement could be due to the simplicity of the model which does not into account of the parasitic elements of the printed circuit board or the discrete components mounted on the board. Another reason is the limitation of the oscilloscope. As its sampling frequency is equal to 500 MHz, it is not able to measure accurately a signal with a frequency superior to 250 MHz. A new model that takes into account the limitation of the oscilloscope is presented in the next part.

7.7 Automatic extraction of susceptibility threshold

The simulation tool proposed by IC-EMC can be controlled manually by the user. The user controls the frequency of the RFI and extracts the forward power for each frequency. This manual process is adapted for an investigation at certain frequencies, but is very long for the extraction of the susceptibility threshold over a large frequency range. That's why IC-EMC proposes an automatic mode. In this mode, both the amplitude and the frequency of the RFI source are swept linearly between two bounds defined by the user.
To launch the automatic susceptibility simulation, click on "EMC→Susceptibility (dBm) vs frequency". The susceptibility simulation interface is in automatic mode by default. Click the item "Automatic Mode", the following screen appears (Fig. 7-26).

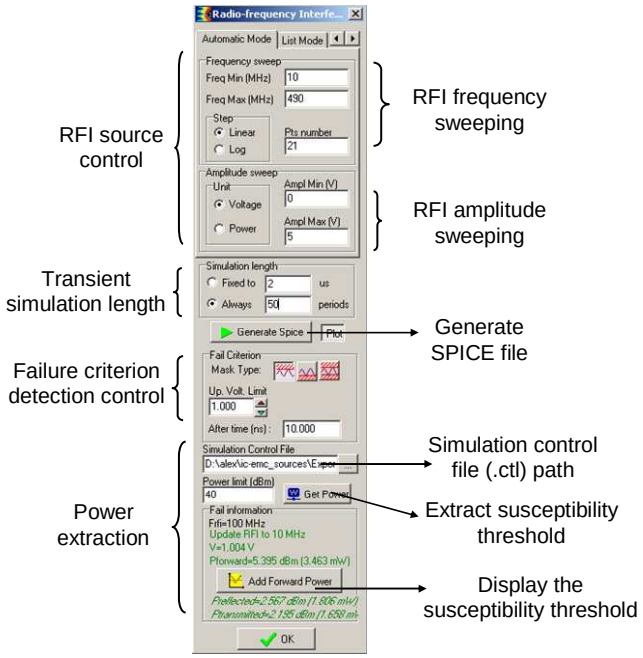


Figure 7-26: RFI control window in automatic mode

In order to describe the susceptibility simulation process in automatic mode, the previous DPI injection on a 330 Ω is reused and improved. A model of a digital oscilloscope replaces the ideal voltage probe (available in the directory ieee\DigOscillo.sym, by clicking on Insert → User Symbol (.SYM)). Open the file "immunity\dpi330ohm\dpi_330_1V_sampling.sch" which is described in figure 7-27. A new symbol has been added after the RC filter of the active probe. This new symbol models a digital oscilloscope which samples the input signal at a given frequency. Figure 7-28 describes the properties of the digital oscilloscope. This symbol is characterized by:

- a sampling frequency Fs, input signal frequency can be reconstructed after sampling only if its frequency is inferior to Fs/2 (Shannon theorem)
- a delay, which shifts the sampling time. In measurement, the RFI signal and the sampling reference of the oscilloscope are never synchronized. However, in simulation, deterministic signals are used so that it is not possible to modify the instantaneous phase between the RFI signal and the sampling reference of the oscilloscope. The delay property offers the possibility to user to evaluate the effect of the phase between the RFI signal and the sampling reference of the oscilloscope.
- a cut-off frequency, the oscilloscope behaves as a first order low pass filter. It models the attenuation of the oscilloscope in high frequency and the image frequency rejection filter.

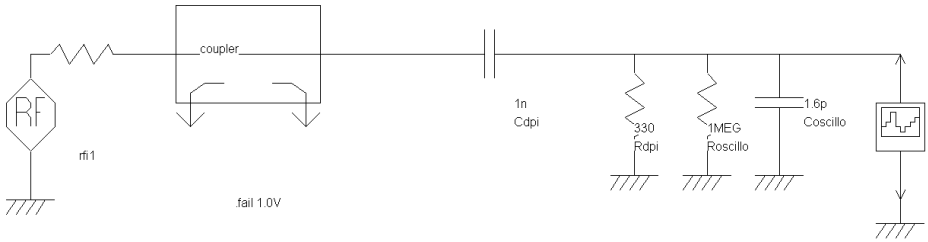


Figure 7-27: Model of a DPI injection on a 330 Ω load – Voltage across the load is done by a digital oscilloscope (immunity\dpi330ohm\dpi_330_1V_sampling.sch)

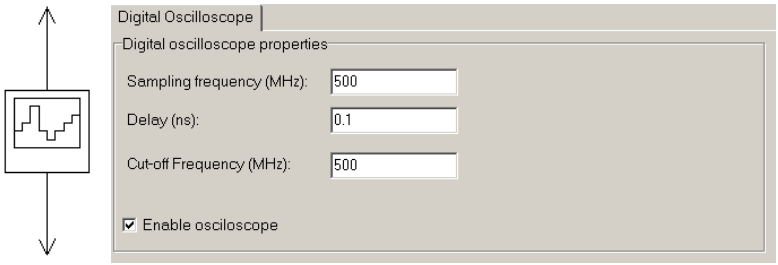


Figure 7-28: Properties of the symbol "Digital oscilloscope"

To simulate the circuit and extract the forward and reflected power, open the susceptibility simulation interface, place the simulator in automatic mode and proceed as detailed below in table 7-5.

Step	Details	Comments
Set the RFI source parameters	Set the frequency linear sweeping from 10 to 490 MHz with 21 frequency points, voltage sweep from 0 to 5 V.	The frequency is swept linearly, so that the susceptibility threshold can be extracted only after one simulation.
Set the transient simulation duration	Set the simulation duration to 50 periods. Select "Always" in the field "Simulation Length" and enter '50' µs. At 10 MHz, the simulation duration is equal to 5 µs, while it is equal to 500 ns at 100 MHz.	For a given simulation transient step, the simulation runs faster at higher frequency for an equivalent accuracy in term of susceptibility level extraction.
Set the susceptibility criterion	Enter the value '1.0 V' in the field "Up volt. limit" in the section "Fail Criterion" of the RFI control interface and click on the button 	The value may be predefined using a label with the syntax ".fail 1.0".
Simulate	Click "Generate Spice". Launch WinSPICE and open the file *rfi_dpi_330_1V.cir*.	
Extract the power	Be sure that the file "RFIcontrol_dpi_330ohms_1V_sampling.ctl" appears in the field "Simulation Control File". Type "30" in the "Power Limit (dBm) field. Type "10" in "After time (ns)" to remove the 10 first ns of the transient simulation from the susceptibility level extraction process. Click "Get Power" to extract the forward, reflected and transmitted powers at each frequency step.	The .ctl file lists all the SPICE simulation result files for the different frequencies. The power limit set a default power value if the susceptibility criterion is not reached. Power extraction process is repeated for the different frequencies.
Extract the power	Click "Add Forward Power" to display the extract susceptibility threshold in the graph "dBm vs. frequency".	RMS values of powers are given. The susceptibility threshold is given in term of forward power.

Table 7-5 : Steps to extract susceptibility threshold in automatic simulation mode

First, the amplitude and frequency sweeping and the transient simulation length have to be configured. Then you launch the SPICE simulation. The principle of the automatic susceptibility simulation is to restart the transient simulation for each frequency. Transient simulation results are written in individual files. A simulation control file "dpi_330_1V_sample.ctl" lists all the transient simulation result files and helps the post-processing tool to locate them. At the end of the simulation, forward power required to induce a failure is extracted at each frequency. The post-processing tool opens successively all the simulation result files and extract the forward power. At the end of the extraction process, the extracted forward power can be displayed. Figure 7-29 presents the extracted forward power and comparisons with measurement.

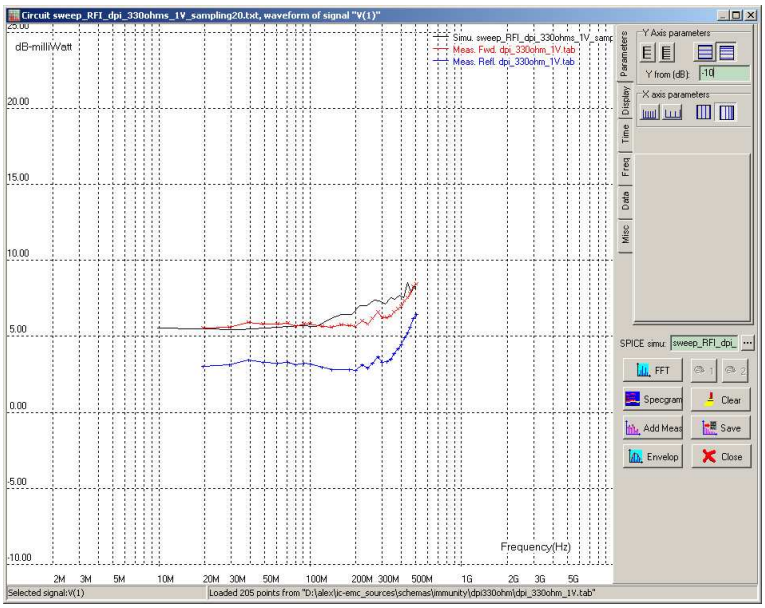


Figure 7-29: Comparison between measurement and simulation of DPI on a 330 Ω load (immunity\dpi330ohm dpi_330_1V_sampling.sch)

The correlation between measurement and simulation is better. Sampling and filtering the signal used to detect the susceptibility criterion contribute to modify the susceptibility level when the signal frequency approaches the sampling frequency.

7.8 Automatic extraction of susceptibility threshold based on List Mode

The automatic simulation mode ensures a fast extraction of susceptibility level as the user has not to repeat the SPICE simulation lauching. However, this mode has one limit when the simulation covers large frequency range and/or the susceptibility level varies a lot with the frequency. In these situations, the RFI amplitude sweep parameters and/or the simulation duration can be optimal for a given frequency range, but not adapted for another frequency range. Moreover, in automatic mode, the susceptibility criterion is assumed to be constant over all the frequency range, which is seldom true. The sensitivity level of a circuit to a voltage disturbance can evolve with frequency. If the automatic mode is used, SPICE simulation has to be configured only for narrow frequency ranges.
A solution to these problems consists in predefining all the parameters for the susceptibility simulation:

- RFI amplitude sweeping (minimum to maximum amplitude)
- SPICE transient simulation duration
- susceptibility criterion given in voltage limit

All these information are contained in a list of susceptibility simulation configurations provided by a text file to the simulator. To launch the list mode susceptibility simulation, click on “EMC→Susceptibility (dBm) vs frequency”. The susceptibility simulation interface is in automatic mode by default. Click the item “List Mode”, the following screen appears (Fig. 7-30).

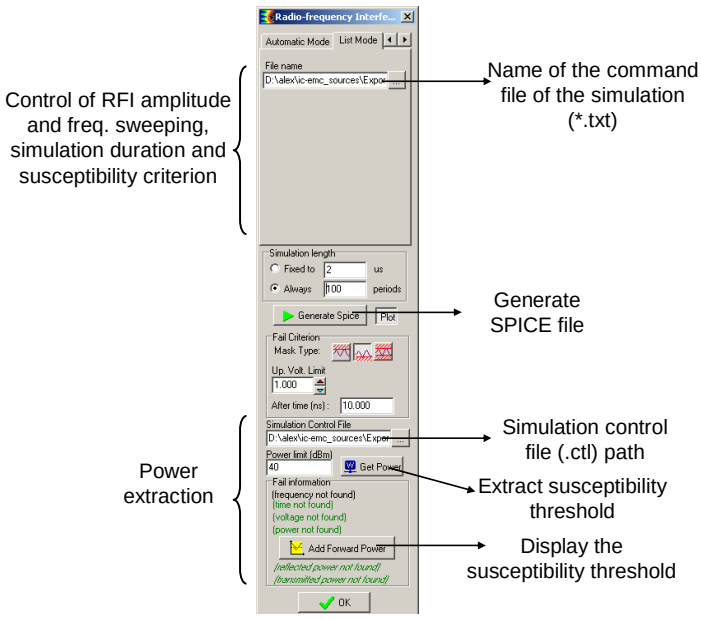


Figure 7-30: RFI control window in list mode

The RFI control panel disappears since the RFI amplitude and frequency sweeping is defined in a text file. The name of this file is given in the field "File name". Select the file "immunity\dpi330ohm\ List_RFI_dpi_330ohm_1V.txt" by clicking on the button ... . This file contains also the transient simulation duration and the susceptibility criterion (only a voltage limit) for each RFI frequency. Figure 31 describes the contents of the list. The format is very simple and can be manually created: a header line which starts with the symbol #, followed by N configuration lines for N RFI frequencies.

```
#Freq_(Hz) Min_RFI_voltage_(V) Max_RFI_voltage_(V) Duration_(µs)
Voltage_Criterion_(V)
10000000    0     2     10    1
20000000    0     2     10    1
30000000    0     2     5     1
50000000    0     2     3     1
80000000    0     2     2     1
100000000   0     2.5   2     1
130000000   0     2.5   1.5   1
150000000   0.5   2.5   1     1
200000000   0.5   2.5   1     1
```

Figure 7-31: Format of the text file for thesusceptibility simulation configurations (immunity\dpi330ohm\ List_RFI_dpi_330ohm_1V.txt)

Launch the SPICE simulation by clicking on the button Generate SPICE. At the end of SPICE simulation, click on the button Get Power to extract the susceptibility level. The information in the fields "Simulation Length" and "Fail Criterion" are ignored since they are given by the text file.

7.9 Summary

In this chapter, simulation methodologies to predict susceptibility of circuits to continuous wave disturbances have been presented. These methodologies are in accordance with the IC susceptibility measurement standards. The simulation process is based on transient simulations and amplitude and frequency sweep of the radio frequency interference source. Extracted susceptibility threshold are given in term of forward power of the disturbance, which require the use of a directional coupler. Following the example of IC emission modeling, the basis of a preliminary standard model called ICIM dedicated to susceptibility of circuit prediction were described. The automatic simulation mode proposed in IC-EMC has also been presented, which features a user's controlled amplitude and frequency swept.

7.10 References

[7-1] IEC 62433-4: "Integrated Circuit – EMC IC Modeling – Part 4: ICIM-CI, Integrated Circuit Immunity Model, Conducted Immunity", New Proposal, 2008

[7-2] IEC 62132-1: "Integrated Circuits – Measurement of Electromagnetic Immunity, 150 KHz to 1 GHz – Part 1: General and Definitions", International Electrotechnical Commission, Geneva, Switzerland, September 2001

[7-3] M. Ramdani, E. Sicard, A. Boyer, S. Ben Dhia, J. J. Whalen, T. H. Hubbing, M. Coenen, O. Wada, "The Electromagnetic Compatibility of Integrated Circuits: Past, Present and Future", IEEE Transactions on Electromagnetic Compatibility, vol. 51, no. 1, February 2009.

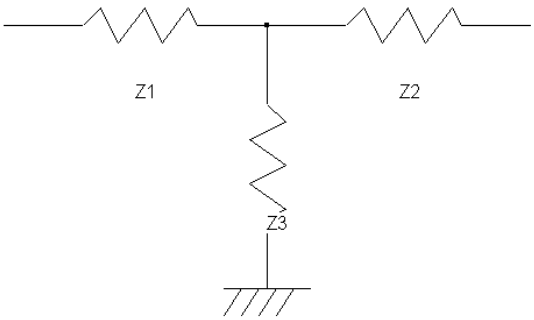
[7-4] A. Boyer, « Prédire la Susceptibilité des Circuits aux Agressions Electromagnétiques », Electronique – Le mensuel des ingénieurs de conception, mars 2008, No 189

[7-5] IEC 62132-4: "Integrated Circuits – Measurement of Electromagnetic Immunity, 150 KHz to 1 GHz – Part 4: Direct RF Power Injection Method", International Electrotechnical Commission, Geneva, Switzerland, 2004

7.11 Exercises

1. Exercise 1 – Attenuator for susceptibility test

Simple models of attenuator can be found in the literature. The following figures and equations propose a T model of attenuator.



$$Z_2 = \frac{L}{1-L^2} Z_C \qquad Z_1 = Z_2 = \frac{1-L}{1+L} Z_C$$

where L is the attenuation of the device (0<L<1), Zc is the input and output reference impedance.

1. Propose the schematic of an ideal 6 dB attenuator based on 3 resistors. The attenuator is 50 Ω adapted at input and output.

2. Verify the properties of your attenuator by a S parameter simulation.

3. Open the file "immunity\exercises\RFI_atten6dB.sch". A conducted RFI source is connected to an unmatched load through a coupler and an attenuator. The frequency of the disturbances is set at 100 MHz. Compute the forward and reflected power in the following cases:

- with an attenuator
- without any attenuator

and compare the results. Why should an attenuator insert in the DPI injection path?

2. Exercise 2 – DPI injection on the power supply of a digital I/O

The susceptibility of a digital output buffer is investigated on the band 1 MHz – 1 GHz. RF disturbances are injected to the I/O power supply pin by a DPI method. The noise coupled on the I/O output signal is measured. The susceptibility criterion is given in term of noise amplitude coupled on the I/O output. The noise margin is equal to +/-20 % of the power supply voltage. The characteristics of the I/O are:

Technology	CMOS 0.25 µm
I/O supply voltage	5 V
Transistor model library	lib\spice.lib
Output buffer model	A simple inverter: NMOS (W=50 µm, L=0.25 µm) PMOS (W=100 µm, L=0.25 µm)
Output buffer equivalent capacitor	Ccomp = 6 pF
I/O decoupling capacitor	Cdec = 100 pF
Package model	R = 0.1 Ω, L = 10 nH, C = neglected
PCB effect	neglected, no external decoupling capacitor
Output load	47 pF capacitor
DPI capacitor	10 nF, ideal
L choke	10 µH, ideal
DPI injection path	Directional coupler, delay = 2 ns
I/O input signal	square signal, freq = 1 MHz, rise/fall time = 5 ns

During this study, noise is measured in three different locations: two external measurements are performed on the power supply pin and across the output load, and an internal noise measurement on the output buffer power supply.
The aim of this exercise is to compare the noise injected at the three test points of the circuit and for the different state of the circuit with an ideal model of circuit and printed circuit board. The results give indications about the penetration of a RF disturbance in a circuit.

1. Build the schematic of the DPI injection of this circuit. Set the RFI frequency to 70 MHz and the amplitude to 1 V. Simulate the noise at the three test points and observe the response. Compare the on-chip and off-chip noise on the power supply for the different output states.

2. Repeat the simulation for the following frequencies: 10 MHz, 50 MHz, 100 MHz, 500 MHz and 1 GHz, and compare the on-chip and off-chip noise on the power supply for the different output states.

3. In order to understand the difference between the power supply noise measured on and off chip, a transfer function of the passive decoupling network (PDN) of the I/O is computed. Isolate the PDN of the I/O (here package and on-chip decoupling capacitor) and connect it to a voltage generator with a 50 Ω serial resistor. Simulate and compare the on and off-chip noise transfer functions. Conclude about the observed differences between the off-chip and on-chip noise. Conclude about the effect of the package at high frequency.

4. In order to understand the difference between the power supply noise between the two output buffer states, the transfer function of the passive decoupling network (PDN) of the I/O is computed for both states of the output buffer. The transistors of the buffer are considered as perfect switch. Build the equivalent model of the PDN with I/O and its output load (neglect the output package effect). Simulate the on-chip noise for both output states. Explain the observed differences between both output states?

5. Simulate the susceptibility threshold of the I/O. Correlate the susceptibility threshold with previous observations.

8 Case Studies

On the IC-EMC website (www.ic-emc.org), several application notes and real case studies can be downloaded. In these case studies, examples of modeling of integrated circuits dedicated to EMC (conducted and radiated emission, conducted susceptibility, near-field scan, power distribution network modeling, package and PCB modeling …) are presented. All these models are built and analyzed with IC-EMC. The different schematic and measurement files are proposed on the the subdirectory "case_study" of the software IC-EMC.

The following list gives a summary of the different case studies (the name of the case study is the name of the subdirectory in "caxse_study") that you can find on IC-EMC website:

- bci_probe: construction of the equivalent electrical model of a BCI probe valid up to 1 GHz
- bga64: BGA package modeling from IBIS file information (the case study is presented in chapter 4)
- cesame: prediction of the near field emission of a digital circuit from ICEM model and comparison with near-field scan measurements
- l4949:
- mpc5534: electromagnetic conducted and radiated emission (EME) modeling based on ICEM of a 32-bit microcontroller designed for automotive purposes
- pa_3g:: structure of a near-field emission model related to a power amplifier used for 3rd generation mobile platform
- pll_pdn: modelling of the power distribution network of a phase-locked loop, in order to predict the amount of conducted interference coupled within the chip
- s12x: description of the full process of construction of emission and susceptibility models for a complex circuit: a MC9S12XDP512 microcontroller from Freescale.
- tqfp100: extraction of parasitc inductance, resistance and capacitance of a TQFP100 package, based on a partial element modelling
- tricore: illustration of the tool ICEM Model Expert, used to construct a first order ICEM model of an advanced 32-bit microcontroller dedicated to automotive applications.

9 Reference Manual

9.1 List of Commands

9.1.1 3D-Package Viewer

The package viewer is based on IBIS information of the integrated circuit. Use the command **"Tools → 3D-Package Viewer"** to display the 3D aspect of the package, including the IOs, IC location and lead-frame structure. When the 3D-package viewer is launched, the tool asks for an IBIS file. The "**Demo**" button displays the IC in 3D with varying observation angles.
Use the X, Y, Z to move the viewer's position in 3D and the light position cursor to change the rendering. The package color and the IC colors are user accessible. The color code for pins is as follows:

- Supply balls are in red (VDD, VCC)
- Ground balls are in blue (GND, VSS)
- I/O balls are in yellow
- Non-connected balls are in Gray

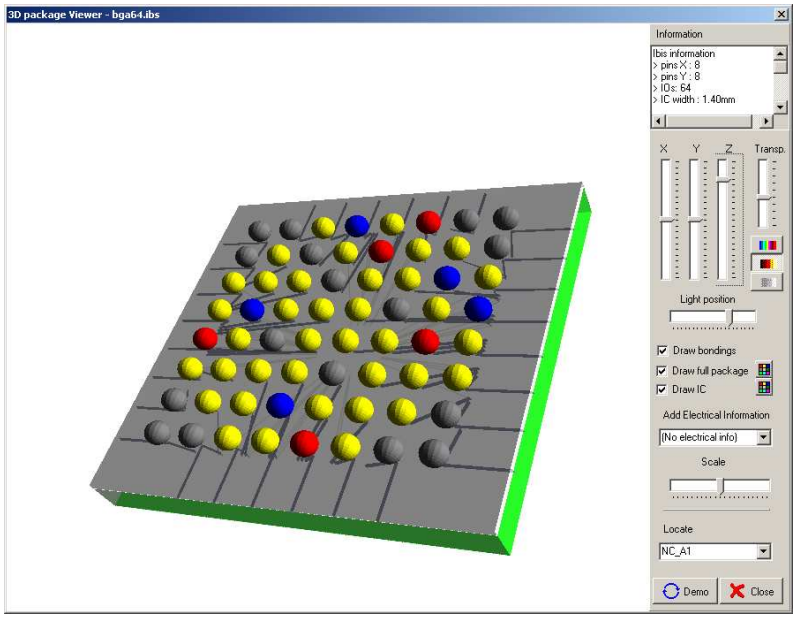


Figure 9-1 : the 3D-package viewer

9.1.2 About IC-EMC

Click on "**Help → About Ic-Emc**". It provides information about the software release and support.

9.1.3 Advanced Package Model

The command "**Tools→Advanced Packaged Model"** opens a tool that helps to automatically generate realistic model of package and compute electrical parasitic elements (R, L, C). The tool proposes several types of packages:

- Dual In Line (DIL), Small Outline Package (SOP): pins placed on both opposite sides of the package. The tool builds automatically a realistic geometrical model from mechanical information.
- Quad Flat Package (QFP): pins placed on all the four side of the package. The tool builds automatically a realistic geometrical model from mechanical information.
- Ball Grid Array (BGA): this type of package is quite complex because the internal redistribution tracks can be placed on several layer. Thus, an automatic geometrical model is not possible. IC-EMC proposes a 3D interface to build the geometrical model, starting from mechanical information.

The interface is composed of three tabs:

- Package generation: the first interface dedicated to the generation or the import of the geometric model of the package. Several mechanical information are required to produce the package model. Appendix H gives details of geometrical parameters. A *.geo file is generated at the end of the package definition, when the button "Generate Geo Model" is clicked. This file contains the geometrical information. If the *.geo file already exists, this file can be directly imported by clicking the button "Import Geo Model". When this tool is opened, only this tab is visible. The two other tabs become visible when a new *.geo has been generated or when a valid *.geo has been imported. Figure 9-2 presents the first tab dedicated to package model definition.

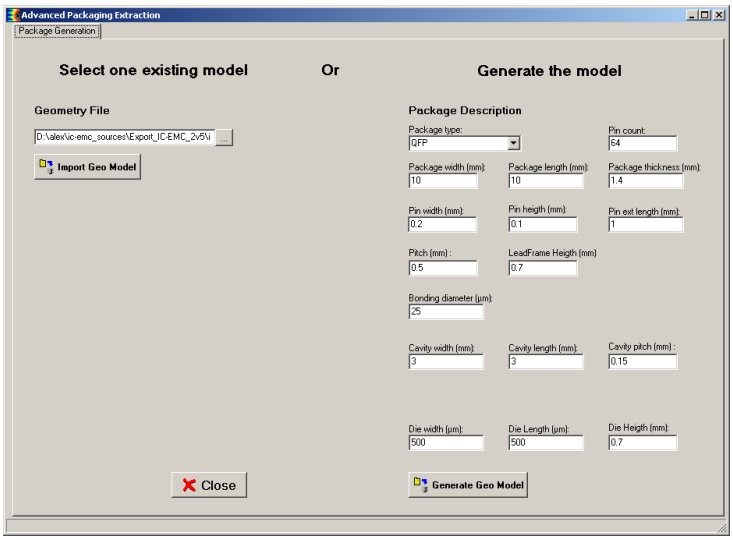


Figure 9-2 : Definition of package model, generation of .geo file

- Model viewer: after a *.geo file has been generated or imported, this tab appears to view a 3D picture of the reconstructed package, as shown on figure 9-3.
- Compute parasitics: this tab is dedicated to the extraction of parasitic resistance, inductance and capacitor of each individual pin of the package. The computation of electrical elements is based on a geometry meshing and a PEEC method. More details can be found in appendix H. Figure 9-4 details the computation interface. First, configure the electrical parameter of the computation: dielectric constant, perfect ground plane presence, frequency, conductivity. Then, select the electrical parameters that you want to extract and finally click on the button "Click" to launch the computation. The simulation duration depends on the size of the package and the number of pins. Resistance extraction is very fast, while inductance and capacitor extraction take a longer time. A progression bar indicates the status of the simulation. At the end of the simulation, you can display the simulation results on the screen on the right. Simulation results for a package model saved as

GEOname.geo are automatically exported in files called GEOname.R, GEOname.L or GEOname.C for resistor, inductor or capacitor extraction respectively.

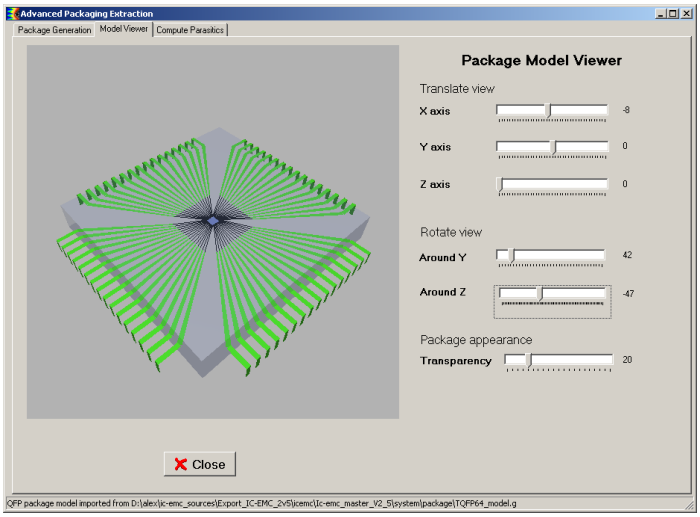


Figure 9-3 : 3D view of the advanced package (package\TQFP64.geo)

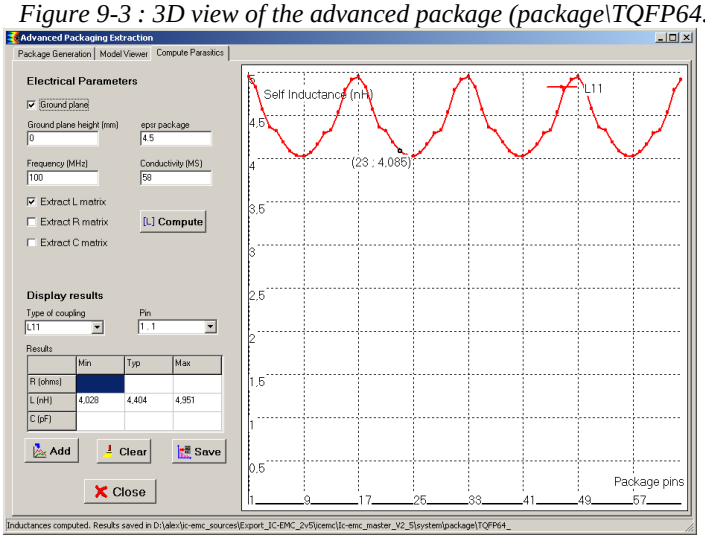


Figure 9-4 : Interface for computation and display of package electrical parasitics (package\TQFP64.geo)

BGA packages are quite complex and the generation of this package type can not be built automatically. Therefore, when the user click on the button "Generate .geo Model" after selecting "BGA" in the field Package Type and typing package mechanical information, a special interface is opened to help user to build a custom geometrical model of a BGA package. More details are given in appendix H.

9.1.4 Advanced Spice & Ibis

The command "**Tools→Advanced Spice & Ibis"** is based on the IBIS data loaded in the schematic editor (see command **File → Load Ibis File**). It may be used to:

- Generate a symbol including the pin list and package shape (**Physical Symbol**)
- Evaluate the R,L,C values for each pin of the package based on physical estimation of the package lead length and bonding length (R,L,C distribution)

- Evaluate the mutual coupling (Mutual Coupling)
- Generate advanced IBIS netlist including accurate evaluations of packge and lead elements (IBIS netlist)
- Generate sub-circuit containing all R,L,C sub-elements in a Spice-compatible format (Spice Netlist).

Notice that the parameters displayed in the menu are issued from hidden IBIS parameters related to the physical dimensions of the IC, the package cavity and package size (See **Ibis File** for more information).

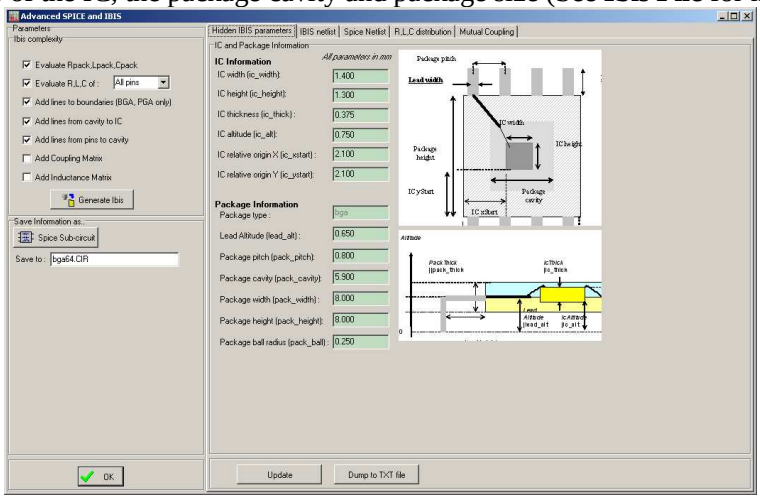


Figure 9-5 : the user's interface for the Advanced Spice and Ibis Information

9.1.5 Another Schema (.SCH)

With the command "**Insert → Another schema (.SCH)**", an existing IC-EMC schematic (*.sch) can be inserted in another schematic.

9.1.6 Attenuation in cables

The command "**Tools→Attenuation in cables"** helps the user to estimate the attenuation brought by cables. Two types of cables are taken into account: bifilar and coaxial cables, that form the main cable categories used in EMC tests. The values of attenuation computed by IC-EMC are based on analytical formulations. It is fundamental to estimate losses brought by cables during emission and susceptibility tests, especially in high frequency where losses can reach several dB. Figure 9-6 describes the interface of the tool. Geometrical and physical information of the cable and frequency must be provided to compute the loss, given in dB/m.

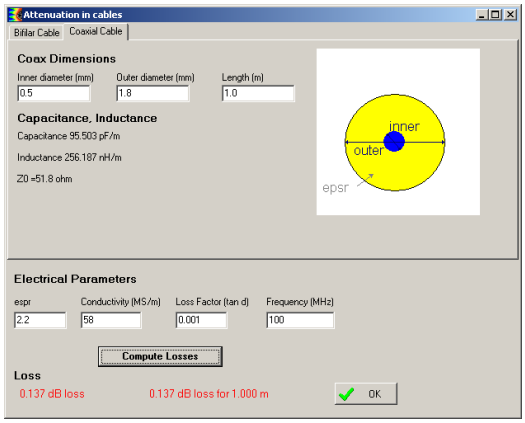


Figure 9-6 : The attenuation in cable evaluation interface

9.1.7 Cavity Model

The tool "**Tools → Cavity Model**" is dedicated to the simulation of Z matrix between several ports placed on a rectangular cavity formed by a power and ground plane pair. The model relies on an analytical cavity

resonator model [9-1] [9-2]. The analytical method is based on the solution of Helmholtz equation with the Green's function for rectangular plane. Figure 9-7 presents the default screen dedicated for power and ground planes dimension and property configuration. The power and ground planes lies on (x,y) plane and are separated by the distance "Thickness". In the table Access Point, the (x,y) coordinates of the input ports are defined. The port shape is assumed square and their width is given in the column "W (mm)". Click on "Add access" to add a new port, or "Remove access" to remove the last defined port. The analytical computation is configured in the screen called "Model Parameters". The maximum cavity resonance orders and the frequency sweeping configuration are defined here. Click on the button Compute Model to launch the analytical simulation. Finally, the results can be plotted on the graph on the right part of the screen, from the screen "Results" (Fig. 9-8).

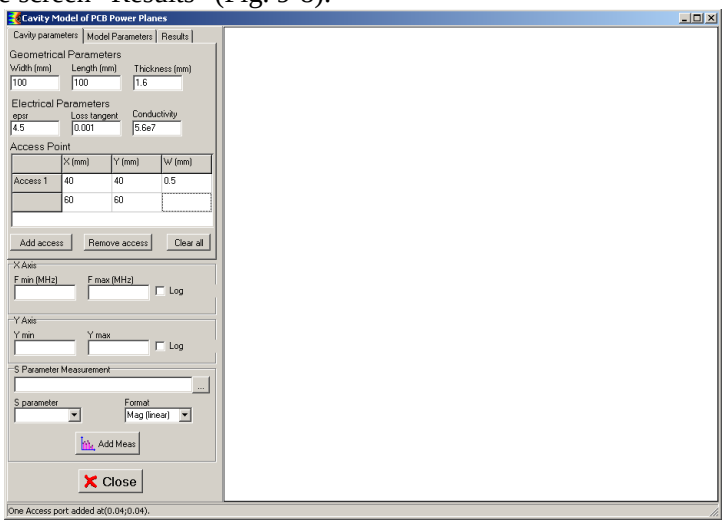


Figure 9-7 : Configuration of cavity dimensions and port placement

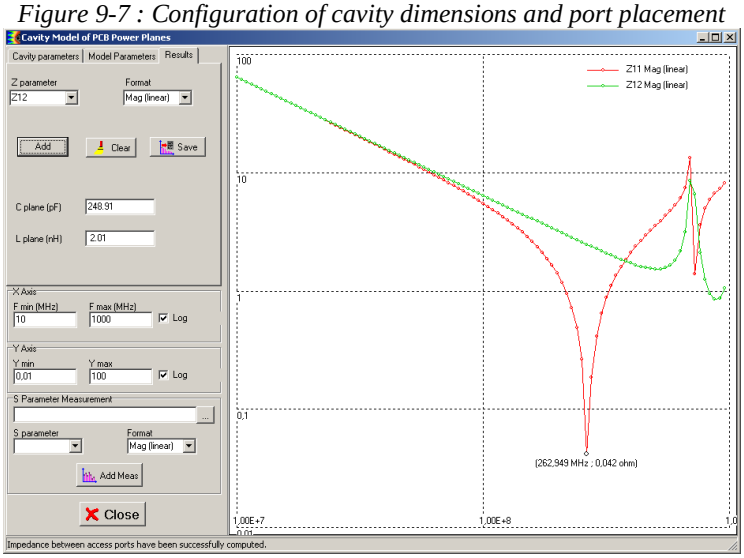


Figure 9-8 : Cavity resonator model: Analytical computation result plot

The Z parameter of the N port matrix can be plotted versus the frequency. The total inductance and capacitance of the power plane are also computed. The Z matrix can be saved in an output file in Touchstone format.

9.1.8 Check Floating Lines

The command "**Tools→Check Floating Lines**" can detect problems of interconnections in the schematic. The schematic diagram is scanned in order to detect interconnects with a wrong connection to the symbol or other interconnects, as in the example of figure 9-9.
The tool "Check Floating Lines" is launched automatically each time the button "Generate SPICE File" is pushed.

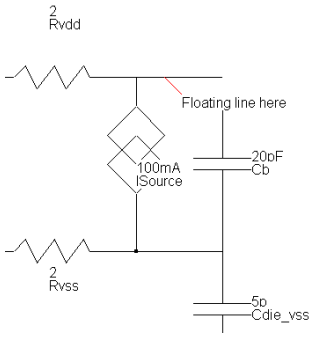


Figure 9-9 : Example of floating line

9.1.9 Connect

Use the command "**Edit → Connect**" command to create the electrical contact between crossing interconnects.

9.1.10 Copy

(CTRL+C)
Click on the Copy icon, or on "**Edit → Copy**". Move the cursor to the design window, and delimit the active area with the mouse. Consequently, all the graphics included in this area are copied. The external shape of the copied elements appears. Fix those copied elements at the desired location by a click on the mouse.
Click on Undo to cancel the copy command.

9.1.11 Cut

(CTRL+X)
Click on the Cut icon or on "**Edit → Cut**". Move the cursor to the design window, and delimit the active area with the mouse. Consequently, all the graphics included in this area are erased. Click on Undo to fix those elements back into the design. One symbol only can be erased by a click inside its shape when the cut command is active. The symbol is then erased. One single interconnect can be erased by a click on its wire when the cut command is active.

9.1.12 dB and unit Converter

A convenient tool has been added to the EMC menu, called "EMC unit converter", to compute the correspondence between linear and dB units. In the example shown in figure 9-8, the value 2V is converted into dB (6.02). A value in dB may be converted into linear scale. Available units are V, A and Watts. For Watts, the log scale is 10.log(Y), and 20.log(x) for the other units.

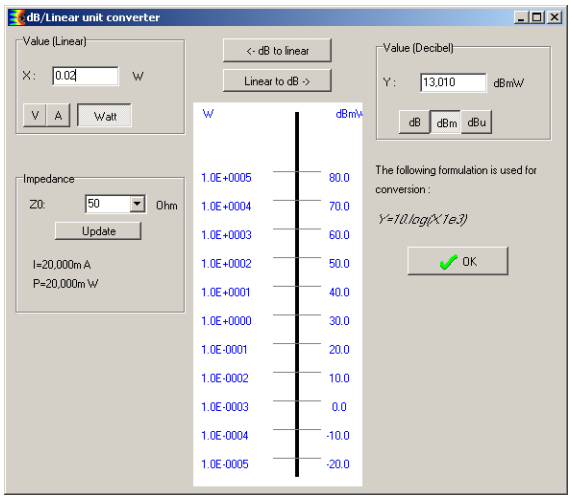


Figure 9-10 : The user's interface for the EMC unit converter

To obtain the current, voltage or power flowing in a 50-Ohm load, click the button "Update". In the example shown in figure 9-10, a 1.0V voltage on a 50-Ohm load results in a 20 mA current and induces 20 mW dissipation.

9.1.13 Electrical Net

 Click on the icon above or on "**View →Electrical Net"**. Then, click in the desired interconnect or pin in the schematic diagram. After an extraction procedure has been carried out, you will see that all the wires connected to that node. Click <Escape> or "**View → Unselect All"** to unselect the diagram.

9.1.14 Emission dBµV vs. frequency

The command "**EMC → Emission dBµV vs. Frequency**" gives access to the following screen. The emission spectrum is the Fourier Transform of the time-domain SPICE simulation store in the file shown in front of "Spice Simu". The X and Y axis may be modified using the icons situated on the top-left corner of the screen. The FFT parameters may be adjusted manually.

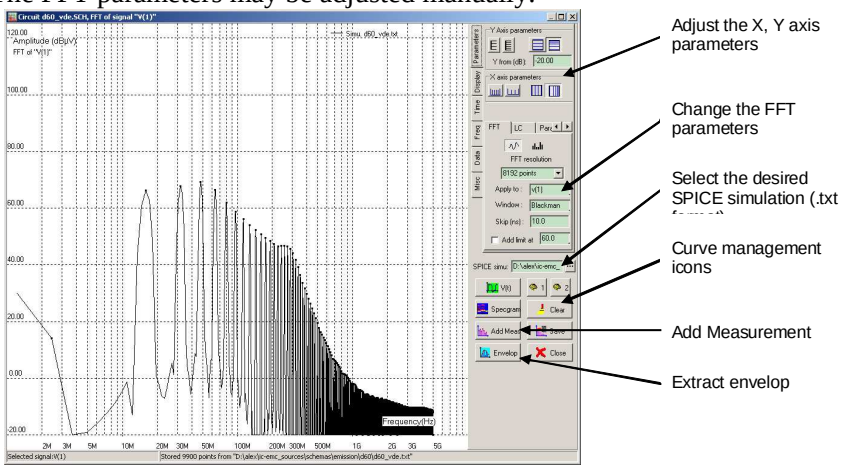


Figure 9-11 : the window "Emission vs. Frequency"

9.1.14.1 Control Buttons

Button	Description
FFT	Compute the fast fourier transform of the selected signal
1 2	Memorizes the current spectrum to “memo curve 1” or “memo curve2” for future comparison purpose
Specgram	Access to the spectrogram of the selected signal
Add Meas	Add a measurement file to compare with simulation. The usual format for measurement is tabulated dBµV vs. frequency (in Hz). See the appendix for more details on measurement file formats.
Save	Saves the displayed spectrum in a text file, two columns : frequency (in Hz) and energy in dBµV
Envelop	Compute the envelop of the active signal. The active signal is selected in the sub-menu “Display → Envelop parameters”.
Close	Close the window and returns to the main screen.

9.1.14.2 Display Sub-Menu

The display sub-menu controls the color and status of four possible spectrum curves:

- The simulated spectrum, computed by applying a FFT to the SPICE time-domain simulation
- The measured spectrum (directly dBµV vs. frequency)
- The memo curve 1
- The memo curve 2

9.1.14.3 LC sub-menu

The LC sub-menu lists all possible combinations of L and C values and the corresponding resonant frequencies. For example, the combination of Lvss and Cd induces a resonance at 79.6 MHz, while the combination of Lvdd and Cb leads to 503 MHz.

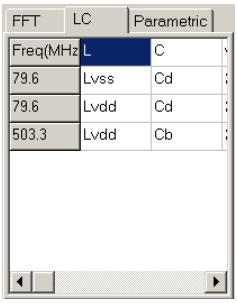


Figure 9-12 : LC sub-menu (emission\d60_vde.sch)

9.1.14.4 Parametric sub-menu

The Parametric sub-menu lists all possible R,L,C elements and enables a direct modification of the value, followed by the generation of the corresponding Spice file. This shortens the parametric investigations on the emission spectrum. In Fig. 9-13, the value of Cb may be changed directly without going back to the

editor window.

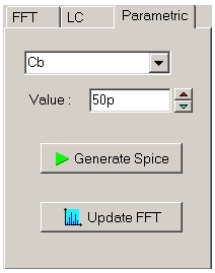


Figure 9-13 : Parametric investigations on a given R,L or C component

9.1.15 Exit IC-EMC

Click on "**File → Exit IC-EMC**" (Or CTRL+Q) in the main menu. If you have made a design or if you have modified some data, you will be asked to save it. After confirmation, you can return to Windows.

9.1.16 Eye Diagram

The command "**Tools → Eye diagram**" opens a special screen for plotting eye diagram for signal integrity analysis. The tool must be launched only if a schematic containing an Eye Diagram symbol (available in ieee\EyeDiag.sym, then click on Insert → User symbol (.SYM)) have been loaded on IC-EMC interface and the associated SPICE simulation result file exist. In these conditions, when the eye diagram tool is launched, the SPICE simulation result file name (*.txt) appears in the field "Simulation Data Source". Click on the button Eye to plot the eye diagram (Fig. 9-14).

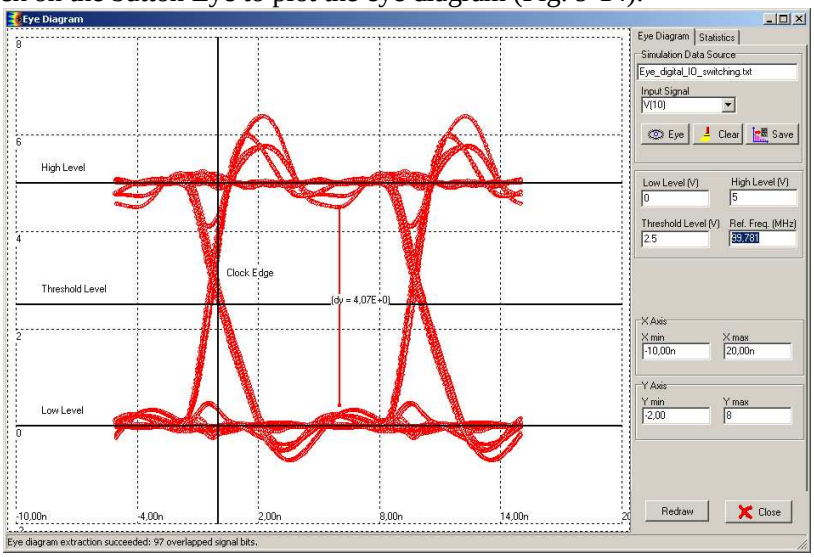


Figure 9-14 : Eye diagram plot (basic\signal_integrity\ Eye_digital_IO_switching.sch)

Remark: only one eye diagram symbol is supported by schematic. All voltage or current probes should be desactivated for eye diagram simulation.

9.1.17 Flip Vertical/Horizontal

To apply a horizontal or vertical flip to one part of the design, click on "**Edit → Flip**". Then, delimit the area inside which the elements will be changed.

9.1.18 Frequency Planning

When non linear devices are excited by several signals, the distorsion of these signals induced by the device behaviour leads to new harmonic content due to intermodulation products. The command "**Tools → Frequency Planning**" offers a simple calculator of frequencies of the new harmonics produced by the intermodulation products between two harmonic excitation signals F1 and F2 (Fig. 9-12). These new harmonics are characterized by two integer numbers (m,n) related the order of the intermodulation product, such that their frequency Fmn is given by:

$$F_{m,n} = \pm m \times F_1 + \pm n \times F_2$$

The frequencies of both input signal are given in MHz, the maximum order for m and n is given in the field Max. Harmonic Index", which is limited to 100. Click on the button Compute to extract the intermodulation product frequencies. The results are displayed in two tables: The "Frequency Planning Array" (on the left) gives the intermodulation product frequency value versus (m,n) couple. The "List of Frequency" (on the right) gives a list of all the new harmonic frequencies in ascending order. Click on the button Save to write both tables in an output file *.txt.

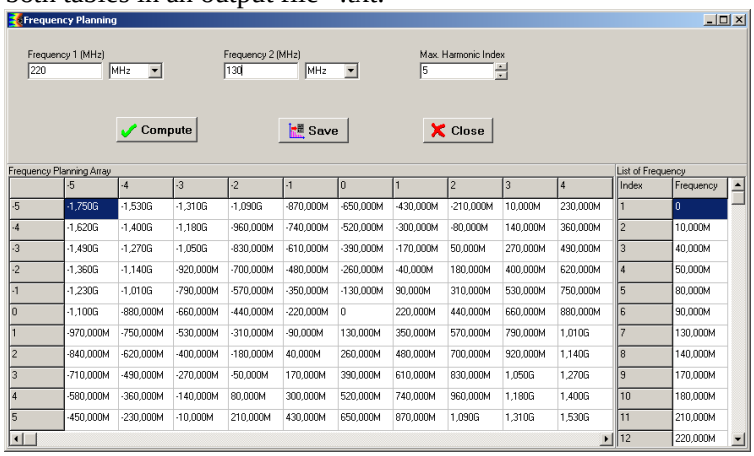


Figure 9-15 : Calculation of the frequencies of intermodulation products between 2 harmonic signasl

9.1.19 Frequency/Wavelength Converter

The wavelength corresponding to a given frequency may be computed in a dedicated screen added to the **Tools** menu and called "**Freq./Wavelength converter**"

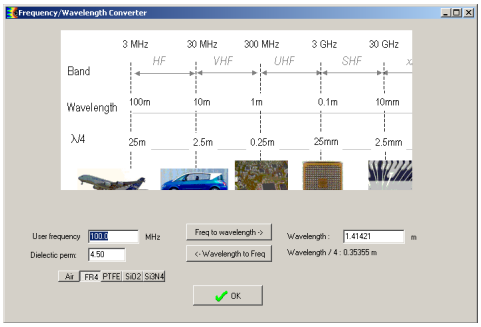


Figure 9-16 : The user's interface for the frequency/wavelength conversion

The formulation used for conversion is as follows: $\lambda = \frac{c}{f\sqrt{\varepsilon_r}}$

Material	Relative permittivity
Air	1
FR4	4.6
PTFE	2.2
SiO2	3.9
Si3N4	7

9.1.20 Generate SPICE File

 IC-EMC converts the SCH schematic diagram into Spice format using a specific interface (figure 9-17), invoked by **"EMC → Generate SPICE file".** The Spice file can be exported to analog SPICE-compatible simulators such as PSPICE or WinSPICE.

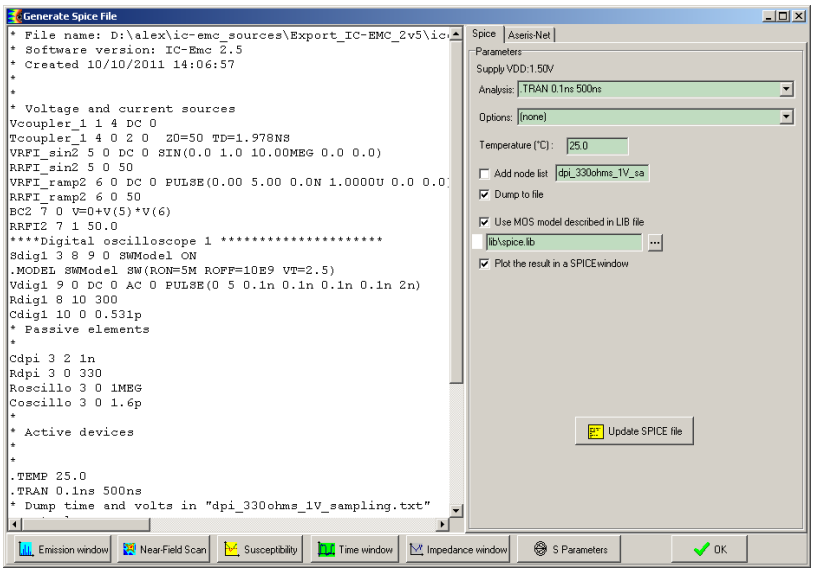


Figure 9-17 : converting a schematic diagram into a SPICE-compatible text file

9.1.21 Generate SPICE sub-circuit

SPICE sub-circuit can be generated from a SPICE schematic containing subcircuit I/Os. Figure 9-18 describes a schematic example with three I/Os placing at device terminals. Click on I/O and give and explicit name.

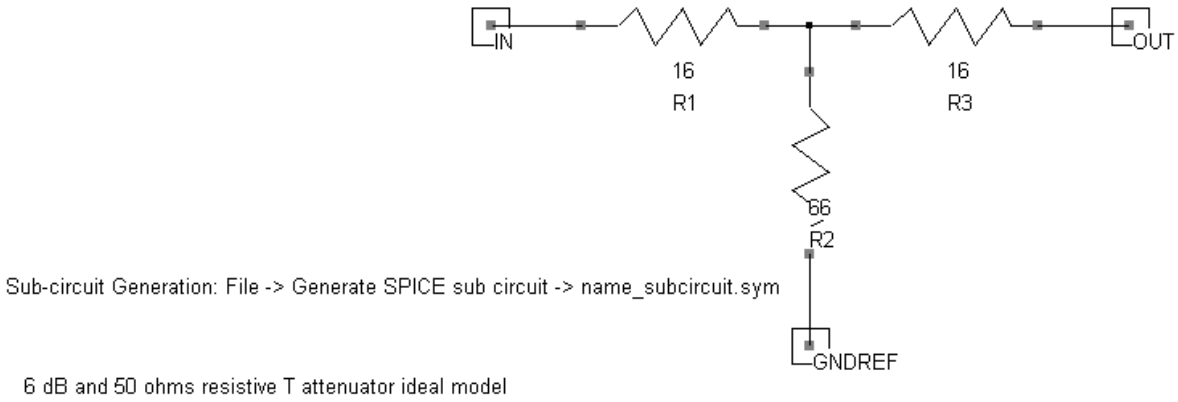


Figure 9-18 : Placement of subcircuit I/O on a schematic to generate a SPICE subcircuit (EMC_lib\attenuator_6dB_subcircuit.sch)

Open the SPICE sub-circuit generation interface by clicking on **"File → Generate Spice sub-circuit"**. The following screen appears. The right part of the screen lists all the I/O of the device and their position (column "Side"), the left part describes the shape of the sub-circuit symbol. The position of I/O can be changed manually by modifying the property Side ('L', 'R', 'T' or 'B' for Left, Right, Top and Bottom respectively) and clicking on the button Refresh. The size of the subcircuit symbol can be updated with the buttons . The subcircuit SPICE description and the graphical symbol are saved in a *.sym file. By default, the name of the *.sym is identical to the schematic name. Change the field "Name" and Save as:" to modify the names of the *.sym file and the SPICE sub-circuit. Click "OK" to generate the *.sym file. Click **"Insert → User symbol"** to add the symbol of the subcircuit in a schematic. If you click on the subcircuit symbol, the SPICE description of the subcircuit is edited.

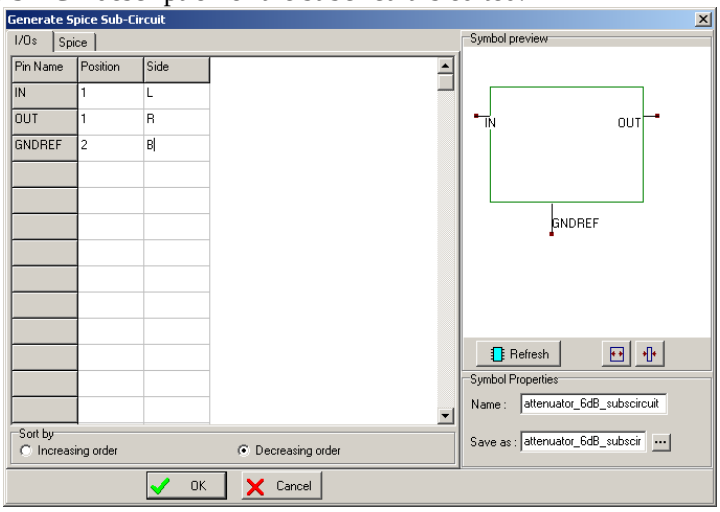


*Figure 9-19 : Generating a SPICE sub-circuit and the graphical symbol, saved in a *.sym file (EMC_lib\attenuator_6dB_subcircuit.sym)*

9.1.22 Help

Provide an on-line help for using IC-EMC. Include a summary of commands, some details about the design rules, and some precision about the current version of the software.

9.1.23 Ibis Interface

The IBIS interface ("**EMC → Ibis Interface**") enables the presentation of IBIS data file (left of figure 9-20), and to control a set of commands related to the exploitation of the IBIS information. The command "**3D Draw**" shows the package in 3D with a user control of the 3D view. The command "**Generate Symbol**" converts the package into an IC-EMC-compatible symbol, with associated pin list and tentative lead frame drawing.

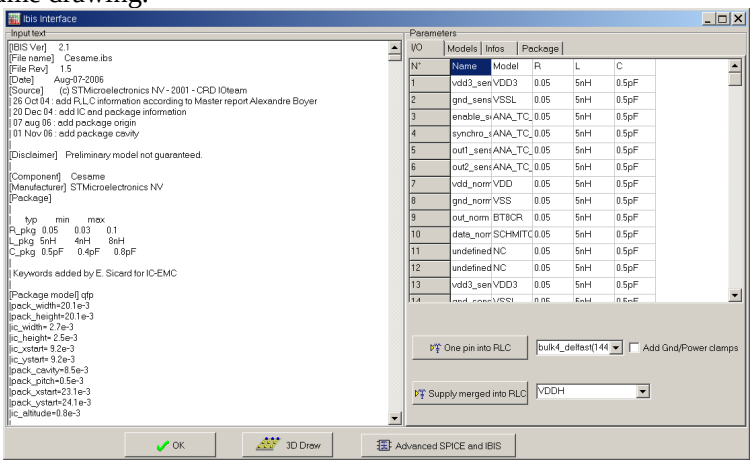
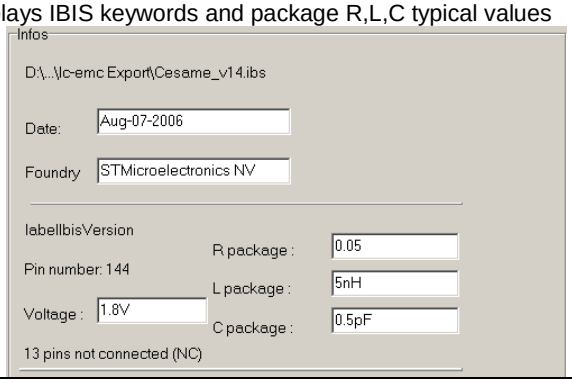


Figure 9-20 : The IBIS window

The other sub-commands are listed below.

Sub Menu	Command	Description
"I/Os"	One Pin Into R,L,C	Choose the desired pin that will be converted into a R,L,C circuit according to the information available in the R_pack, L_pack, C_pack variables of the [Package] sub-section.
	Supply Merged into R,L,C	Choose the desired supply model. All pins with the associated model will be converted into a R,L,C circuit according to the information available in the R_pack, L_pack, C_pack variables of the [Package] sub-section. The resistance will be divided by the number of pins, as well as the inductance. The capacitance will be multiplied by the number of pins.

Sub Menu	Command	Description
"Models"	Y axis	Change the Y scale
	From A, to A	Manually define the Y axis boundaries
	Draw	Redraw the I/V current
	Dump	Save the I/V curve in a ibis-compatible format
	PU	Draw pull-up I/V information if available
	PD	Draw pull-down I/V information if available
	Pc	Draw Power-clamp I/V information if available
	Gc	Draw Gnd-clamp I/V information if available
	RW	Draw rising-waveform V(t) if available
	FW	Draw falling-waveform V(t) if available
	Add Data	Add a simulated I/V or V/t from a Spice simulation to compare with the current I/V or V/t from IBIS. The "TXT" format assumes 3 columns (index, voltage, current), the "DAT" format assumes 2 columns (voltage, current).
	-Sign	Changes the sign of the loaded data through command "Add Data"

Sub Menu	Command	Description
“Info	None	Displays IBIS keywords and package R,L,C typical values 

Sub Menu	Command	Description
Package	I/O color	Changes the I/O color in the 2D-view of the package
	Background Color	Changes the I/O color in the 2D-view of the package
	Display coordinates	Adds the [x,y] numbers or letters to the 2D-view
	Display names	Add all package pin names to the 2D-view
	Locate Pin	Select the desired pin which will appear in purple in the drawing, with an estimation of the 2D-position
	View	Top view or rear view. By default, top view.

9.1.23.1 Hidden Physical Information

Some important information is resourced in the IBIS file related to the package and IC physical dimensions. The information is placed in the [Package model] section, and starts by « | » to avoid parsing errors with conventional IBIS loaders. The physical dimensions are very important information to rebuild the lead frame structure of the package, together with the bonding structure and access to the die.

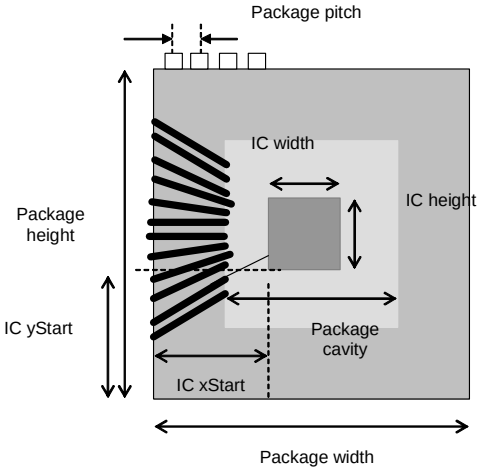


Figure 9-21 : Top view of the package

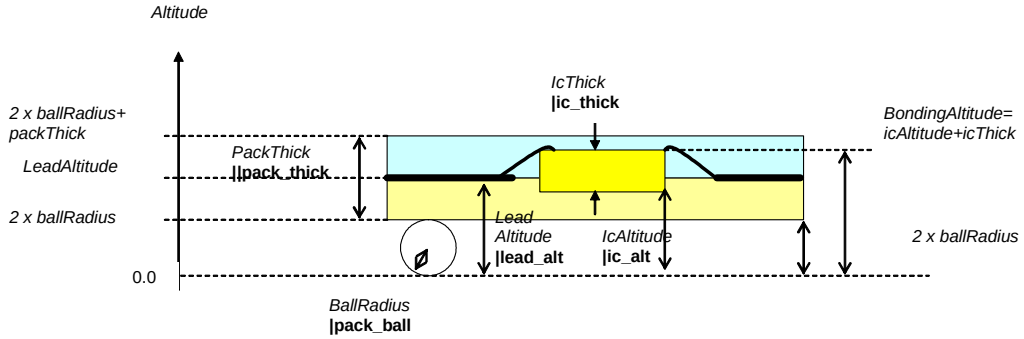


Figure 9-22 : Cross-section and main physical parameters describing a package

Hidden parameter	Description	Example
pack_width	Package width	20.1e-3 m
pack_height	Package height	20.1e-3 m
ic_width	Die witdh	6.55e-3 m
Ic_height	Die height	6.33e-3 m
ic_xstart	Die location in X related to the package	6.73e-3 m
ic_ystart	Die location in Y related to the package	6.84e-3 m
ic_thick	IC thickness	500e-6
pack_pitch	Package pin pitch	0.5e-3 m
Lead_alt	Lead altitude over ground plane	0.5e-3 m
ic_altitude	Die altitude over the ground plane	0.8e-3 m
Pack_ball	BGA ball radius	0.25e-6 m

Table 9-1 : Hidden parameters stored in the [package model] section

9.1.24 ICEM Model Expert

Click "**Tools → ICEM Model Expert**" to access the interface reported below.

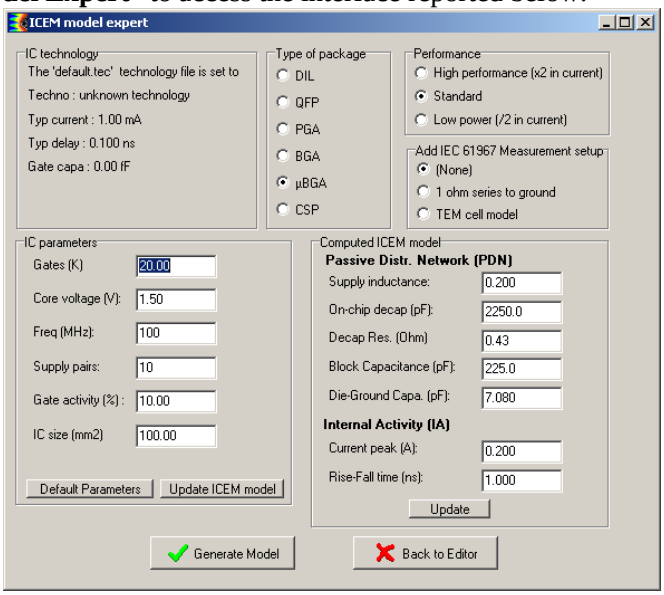


Figure 9-23 : The ICEM model generator and its user's interface

On the left upper corner of the window, the default technological parameters are listed. These parameters are provided in the configuration file "default.tec", which is described in the appendix B. The parameters worth of interest are:

- The typical switching current per gate (0.2 mA in 0.12 µm technology)
- The typical duration of the gate switching (50 ps in the above example)
- The default gate decoupling capacitance (5 fF)

The next menu, called “Type of package”, selects the family of package, which has a direct impact on package inductance. The “performance” menu tunes the current peak (Ib) by increasing the peak current by 100% in “high speed” mode as compared to standard mode. In “low power” mode, the current is reduced by 50%.

In the lower left corner, several parameters that have a direct impact on the ICEM model are given:

- The number of gates (20 Kgates by default)
- The core voltage (1.2 V by default in 0.12 µm)
- The operating frequency (100 MHz by default)
- The supply pairs (Number of VDD/VSS pins, 10 by default)
- The % of switching activity in each active edge of the clock (10% by default)
- The IC size in mm (10 x 10 mm by default)

The computation of the ICEM elements is performed using the approximations described in table 5-6.
The button “Update ICEM Model” updates the proposed values for the Passive Distribution Network and the Internal Activity. The button “Generate Model” creates a simple schematic diagram from these parameters.

You may also add:
- A 1-Ω serial resistance on the ground path, associated with 50-Ω adaptation as defined in the IEC standard “1/150Ω conducted measurement method”. A probe is placed at the location of the measurement system, usually a spectrum analyzer.
- A capacitance/inductance coupling with the septum of the TEM cell, associated with 50-Ω terminations, as defined in IEC standard “TEM radiated measurement method”. A probe is placed at the location of the measurement system, usually a spectrum analyzer.

Ldie_vdd = sqrt(icSurface) *inductanceFactor; Rdie_vdd = sqrt(icSurface) *resistanceFactor;	The serial inductance and resistance are proportional to the width of the die. The factors are around 0.1, if the IC size in in mm.
imax=icPerfo*Gates*typ_current* Gate_Activity/spreadFactor;	The peak current of the source Ib is compute using several parameters: the spread factor is around 10; icPerfo is equal to 2 for high performance, 1 for standard and 0.5 for low power option.
tr := typ_Delay*SpreadFactor;	The rise and fall time of the current source is multiplied by the spread factor.
Lpack_vdd :=L_package/SupplyPairs;	The serial inductance is divided by the number of pairs. The inductance per pin depends on the package technology (15 nH for DIL down to 1nH for CSP).
Cd := Gate_Capa*Gates+ icSupplyPairs*ioCapa+ icSurface*SurfaceCapa;	The decoupling capacitance is the sum of the gate capa, the Io capa and the die surface capacitance.
Cb := Cd/10	The local block capacitance Cb is 10 times lower than the total capacitance
defaultRcd = 1.0; // (Ohm) Decap_Res := defaultRcd/ln(icSupplyPairs)	A parasitic serial resistance is added to the decoupling capacitance to account for interconnect access to physical resistance.
Cdg:= eps0*icSurface*packEpsr /icAltitude;	The die-to-ground capacitance is computed using a simple surface capacitance formulation, given physical parameters such as the surface of the die, the relative permittivity of the package and the IC altitude to ground.
CxFactor = 1fF/mm^2; Cx:= CxFactor*icSurface;	For TEM cell coupling, we use a value Cx which accounts for the coupling between the silicon die and the septum plate, which is the order of 1fF/mm^2

Table 9-2 : Algorithm for ICEM model automatic generation

9.1.25 Impedance vs. Frequency

The command "**EMC → Impedance vs. Frequency**" gives access a specific screen for comparing measured and simulated impedance versus frequency. The simulation file is the result of a frequency-domain simulation controlled by a [Z] element. No FFT is used here as the simulation is directly conducted in AC mode.

Figure 9-24 shows the screen "**Impedance vs. Frequency**". The X and Y axis may be modified using the icons situated on the top-left corner of the screen. An example of comparison between measured and simulated impedance is proposed below.

The measurement file format is usually based on a description of [s]-parameters. Two types of [s]-parameter data files: the ".s2p" and the ".s50" can be imported. See appendix A for more information about how the impedance Z(f) is computed from the [s]-parameter information.

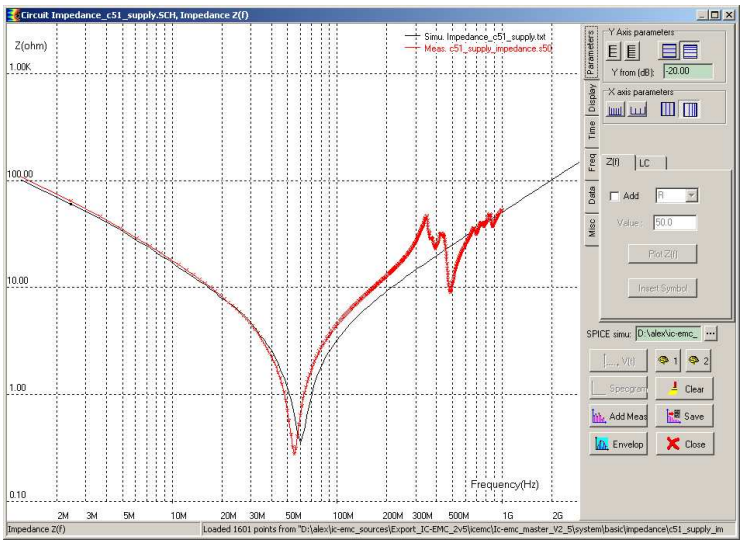


Figure 9-24 : the Z(f) screen with frequency-domain simulations compared to measurements

9.1.26 Insert another Schema

The command "**Insert → Another Schema (.SCH)**" is used to add a SCH file to the existing files. Its content is fixed at the right lower side of the existing schematic diagram. The current file name remains unchanged.

9.1.27 Insert Lib

The command "**Insert → Insert Lib**" allows the selection of a *.lib file through a Windows explorer windows (Fig. 9-25). *.LIB files contain library of device models and parameters (diodes, transistors, transmission lines…). It is necessary to include the library path name and file name in an IC-EMC schematic which include a component with a model declared in a library file.
An other method to include a library in an IC-EMC schematic consists in writing on the schematic a text line (with the command "**Edit → Text**") such as :
".lib path_name\file_name.lib"

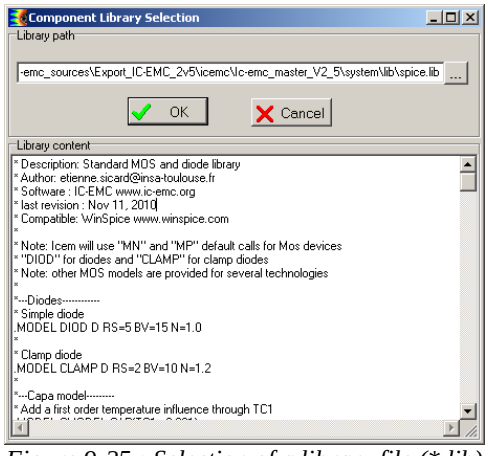


Figure 9-25 : Selection of a library file (.lib)*

A default library is provided in 'lib\spice.lib'. Any library file can be imported, only if it is compatible with WinSPICE syntax (refer to WinSPICE documentation).

9.1.28 Insert User Symbol

The command **Insert → User Symbol** is used to add a user defined symbol to the existing schematic diagram. The user symbol is created using the command "**File → Schema To new Symbol"**. The inserted symbol can be fixed at the desired location.

9.1.29 Interconnect Parameters

The "**Tools → Interconnect parameters**" tool included in the Tool menu computes the R,L,C parameters of an interconnect based on its physical dimensions. Analytical formulations are used for these evaluations (See appendix G for more details about used formulations).
First, select the interconnect types by choosing the adequate cross section. Enter the information about geometry and materials of the interconnect. Then, click on "Apply y=f(x)" to apply analytical formulations to compute the different electrical parameters of the interconnect (resistance, capacitance, inductance per unit length, characteristic impedance, skin effect, propagation delay, loss). Finally, an SPICE equivalent model of the interconnect made of RLC cells can be automatically built. Enter the limit frequency of validity of the model (field "Freq (GHz)") and click on the button "SPICE Model". Automatically, the equivalent SPICE schematic is displayed on the main screen of IC-EMC. You can also give geometrical coordinates to inductances of interconnects to perform near field emission simulations, by selecting the option "Near Field Analysis".

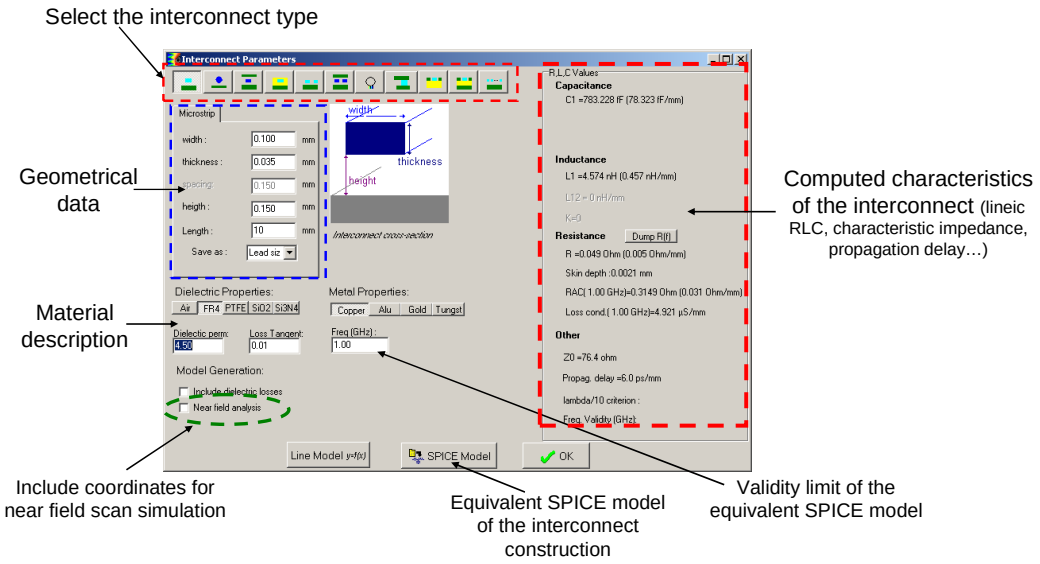


Figure 9-26 : Interconnect R,L,C model based on physical dimensions

9.1.30 LC Resonant Frequency

The command "**Tools → Resonant Frequency**" tool proposes a menu to compute the impedance of L, C at a given frequency. The LC resonance is also computed, with its associated characteristic impedance (Figure 9-27).

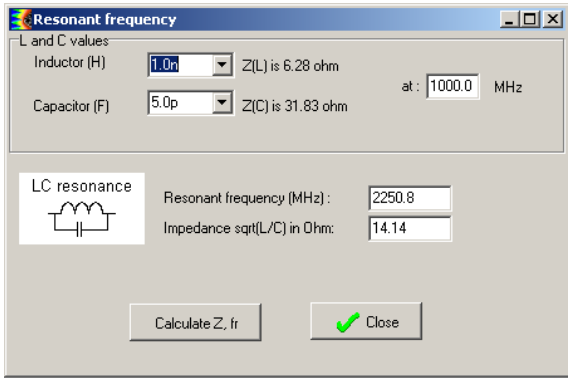


Figure 9-27 : Resonant frequency of given L and C, with associated impedance

Note 1: when you click successively in L and C components, the corresponding resonant frequency is computed and a message appears at the bottom of the main screen.

Note 2: An exhaustive list of resonant frequencies is computed in the Emission window, sub-item "LC". All L and C components found in the schematic diagram are combined to compute resonant frequencies, which are listed by increased frequency.

9.1.31 Line

 (Or right click with the mouse)
The " Line " icon is the default icon. It creates an interconnection between two points in the schematic diagram. If the " Line " icon is not selected, click on it. Then, move the cursor to the display window and fix the start point of the interconnect with a press of the mouse. Keep pressed and drag the mouse to the interconnect end. Release the mouse and see how the line is created.

9.1.32 Load Ibis File (F4)

Command "**File → Load Ibis File**". See "Ibis Interface".

9.1.33 Monochrom/Color (F5)

The command "**File → Monochrom/Color"** switches to monochrome mode: the layout is drawn in black and white. This type of drawing is convenient to build monochrome documentation by avoiding a black background. Alternatively, press "Alt"+"Print Screen" to copy the active window to the clipboard. Then, open Microsoft Word™ or WordPad, click "**Edit→Paste**". The screen is inserted into the document.

9.1.34 Move

To move one graphical element, click on the "Move" icon or **"Edit → Move"**. Then using the mouse, draw an area that includes the elements. Then, drag the mouse to the new location and release the mouse. As a result, the elements are moved the new place. One single line can be moved or stretched (depending where you click) by a direct click on the line. One single text can be moved by a direct click on the text location.

9.1.35 Near-field scan

The command "**EMC → Near-Field Scan**" gives access a specific screen for comparing measured and simulated near-field scan. The simulation file used for simulation is the result of a time-domain simulation where one or more indutances are assigned physical coordinates. The time-domain simulation result is the current flowing in each declared inductance. An FFT is performed on each current information I(t) to compute the corresponding I(f). Each inductance is associated a radiating current element that is represented in the [x,y] plan as an elementary line (see figure 9-28).

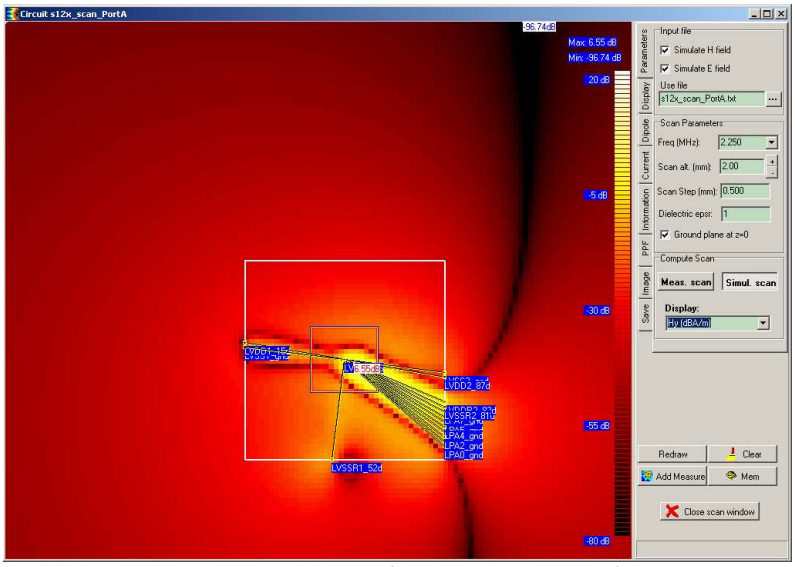
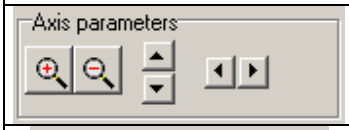
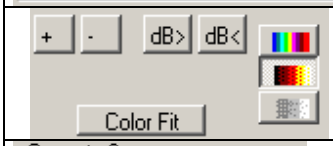
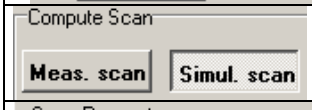
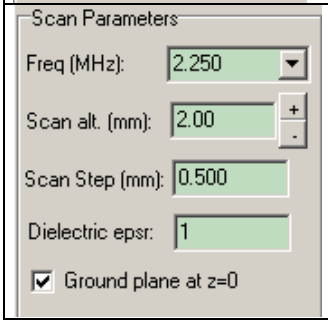
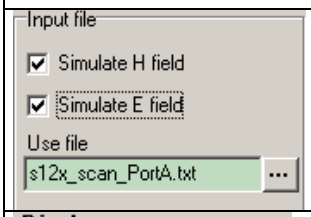
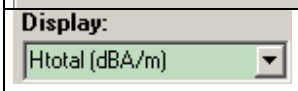


Figure 9-28 : the near-field scan user's interface (case_study\s12x\s12x_scan_porta.sch)

9.1.35.1 Control Buttons

Buttons	Description
	Zoom and shift the near-field scan information
	Adjust the color palette, change the display mode from color to gray levels.
	Switch from measured to simulated scan. When clicking "simulate scan", the EM field is recomputed for all declared current elements, at the given frequency and given altitude.
	The near-field simulation may concern the total magnetic ann electric fields Htotal and Etotal, and also one of its component (along x, y and z axis). The scan altitude may be changed. Click again "Simul. Scan" to recompute the new scan. The frequency of interest may also be changed. Once the new frequency has been fixed, click "Simul. Scan". The new *I(f)* will serve for the scan simulation. The scan step changes the computation step. As the scan area is set to 150 mm per 150 mm, for a 0.5 mm scan step, near field is computed at 90000 points.

	An infinite perfect ground plane can be added below the IC at Z=0.
	Select the scan simulation file which include the current I(t) (*.txt) for each current element associated to each “radiating inductance” or “radiating interconnect” involved in the scan simulation and the voltages at each terminals of inductances. Check the box “Simulate H field” and “Simulate E field” to enable either H field or E field simulation.
	Select the E or H field component to display (x,y,z, tangential and total field component). Magnetic fields are plotted in dBA/m and electric field in dBV/m.
	Add a measured scan. Three ways to described measured scans are supported by IC-EMC: 1. The proposed std format in XML (.XML) 2. The format used by IZM germany (.IZM) 3. The format used by N7 france (.LEN7) See Appendix A for more details about these formats

9.1.35.2 Scan Difference

Several scans can be compared using embedded mathematical operations in the “Evaluate” menu. The results shown below concerns the subtraction of two magnetic field scans, one from simulation and one from measurements. The steps are as follows:

1. The first scan is loaded and stored in memory (Button “Memory”)
2. The second scan is loaded. By a click on “Active-Memory (abs)”, the absolute difference between the active XML scan and the memorized scan appear. The formulation is as follows, for each [x,y] point.

$$difference[x, y] = active[x, y] - memory[x, y]$$

3. An alternative subtraction may be performed based on weighted difference. The algorithm is as follows:

$$weight[x, y] = (\max(active[x, y], memory[x, y]) - dB\min)/(dB\max - dB\min)$$

$$result[x, y] = weight[x, y].difference[x, y]$$

Where
dBmin is the minimum value of the active scan data
dBmax is the maximum value of the active scan data.

9.1.35.3 Other features

- You may add radiating elements using the right button of the mouse.
- When clicking on the [x,y] plane, the value in dBµV at the cursor location is added to the picture
- In the “Current” sub-menu, you may observe the time-domain and frequency domain of the current for each declared current element
- The scan may be configured using a text placed anywhere in the design, starting by keyword ‘.SCAN’. The four parameters that can be listed are given below (See figure 9-29).

.SCAN	Scan configuration	. scan 1e-3 10e6 3.5e-3 2.1e-3	Scan step (1e-3), scan frequency (10 MHz), scan altitude (3.5 mm) and dipole altitude (2.1 mm)

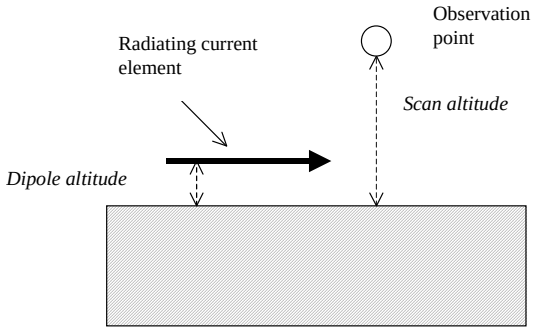


Figure 9-29 : The radiating element, its altitude and the scan altitude

9.1.36 New

Click on "**File→ New"** in order to restart the software with an empty screen. The current design should be saved before asserting this command, as all the graphic information will be physically removed from the computer memory. No Undo is available to disable the New command.

9.1.37 Open (F3)

Click on the icon  . In the list, double-click on the file to load. " .SCH " is the default extension that corresponds to the schematic diagrams.

9.1.38 Parametric analysis

The command "**EMC → Parametric analysis**"  opens a screen for the configuration of a parametric analysis (Fig. 9-30).

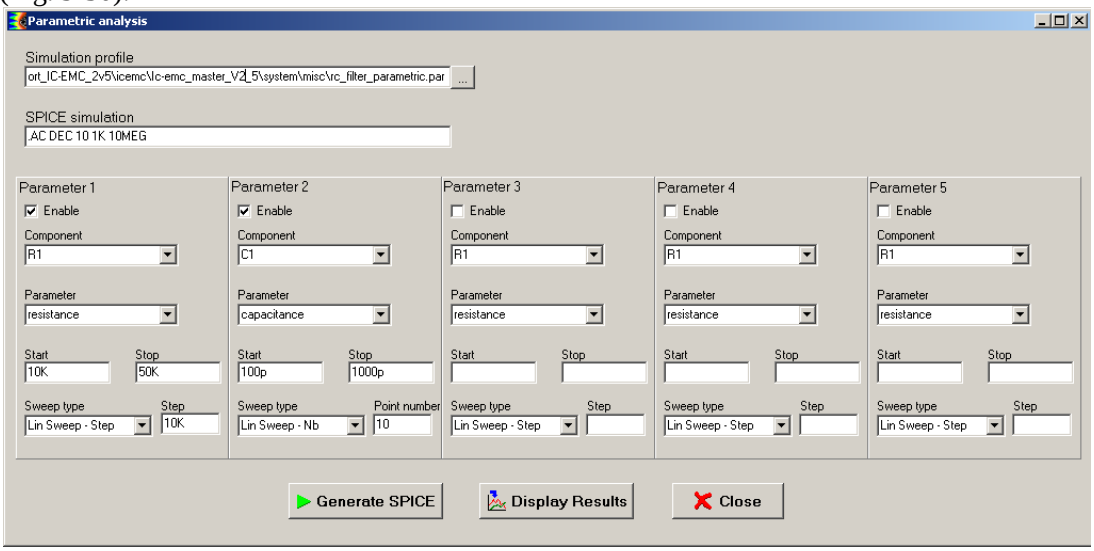


Figure 9-30 : Parametric analysis configuration interface (misc\rc_filter_parametric.sch and misc\rc_filter_parametric.par)

The parametric analysis consists in sweeping one to five parameters of the devices inserted in the schematic (passive or active devices, sources, temperature, model parameters included in a library (*.lib)). Select the option “Enable” to activate a parameter, select one component in the field ‘Component’ (e.g. the resistance R1 of the schematic ‘misc\rc_filter_parametric.sch’ as shown in Fig. 9-30) and one of its property in the field ‘Parameter’ (e.g. the resistance value). Then, define the sweeping with the start and stop value, the type of sweep (Linear or logarithmic sweep, number of step (‘Point number’ field) or value of the step (‘Step’ Field)). Once all the parameters have been configured, click on the button ‘Generate SPICE’. A simulation type has to be preconfigured or detailed in the field ‘SPICE simulation’. Only AC, DC and transient simulation are supported. Although S parameter, susceptibility, emission and near-field scan simulations rely on AC, DC or transient simulations, they are not supported by the Parametric analysis tool.

The parametric analysis configuration is saved in a *.par file, defined in the field ‘Simulation profile’. This file is also required to find all the SPICE simulation result files corresponding to the sweep of the parameters. Each time the button “Generate SPICE” is pushed, the *.par file is updated. The name of the *.par must be the same as the schematic name (for example, for the schematic called ‘misc\rc_filter_parametric.sch’, the configuration of the parametric analysis is saved in the file ‘misc\rc_filter_parametric.par’). A pre-existing parametric analysis file can be imported by clicking on the button  .
At the end of the SPICE simulation, click on the button ‘Display Results’ to plot the simulation results vs. parameter values (Fig. 9-31). The parametric analysis configuration file *.par can be loaded in the field ‘Simulation Data Source’. Select the different parameter values and click on the buttons Add or Clear to add or remove simulation curves. The simulation curves can be saved in a *.txt file. Measurement can be loaded in a *.tab format.

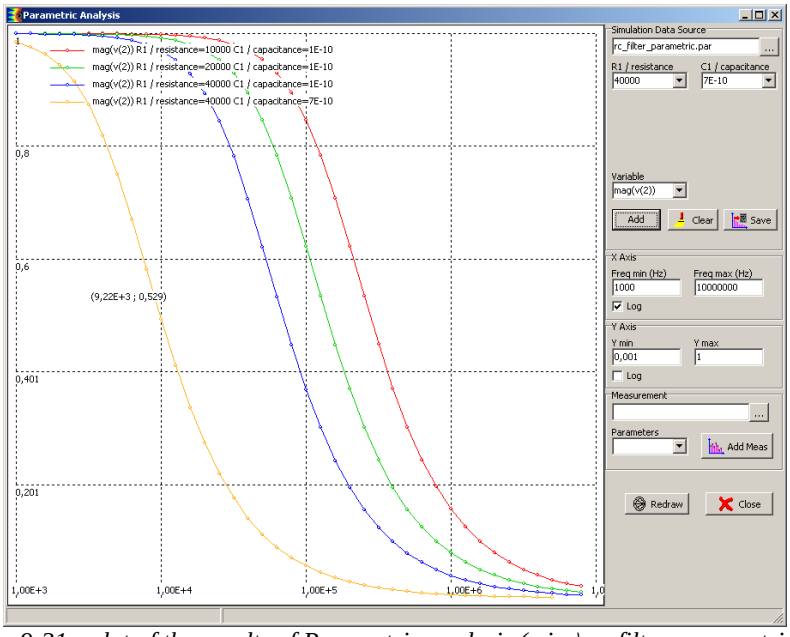


Figure 9-31 : plot of the results of Parametric analysis (misc\rc_filter_parametric.par)

9.1.39 Paste (CTRL+V)

Invoke the *Paste* command “**Edit→ Paste”**. All previously copied elements are pasted at the desired

location. Deleted elements can be replaced that way. Click "**Undo"** to cancel the *paste* command.

9.1.40 Patch Resonant Frequency

The "patch" is a low gain, narrow-bandwidth antenna. Many types of vehicles concerned with aerodynamic considerations require such type of low-profile antennas. Typically, a patch consists of a thin conducting sheet about λ by ½ λ mounted on a substrate and isolated by a dielectric. The patch-to-ground-plane spacing is usually around λ/100. The patch length is designed based on the desired resonance with W=λ, while L is often constrained by availability of space in the electronic device. A practical choice of L is λ/2. A larger L would increase efficiency but higher order modes might distort the radiation patter.

The formulation for the resonant frequency of the patch antenna depends on its physical dimensions W and L, as follows:

$$f_{mn} = \frac{1}{2\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m}{L}\right)^2 + \left(\frac{n}{W}\right)^2}$$

where

fmn=frequency (Hz)
ε= permittivity = $\varepsilon_0\varepsilon_r$
ε_0= $8.85x10^{-12}$ F/m
ε_r= 3.8 (SiO2)
μ= permeability= $\mu_0\mu_r$
μ_0= $4\pi.10^{-7}$ H/m
μ_r= 1 (Air)
m=mode (integer 0,1,2..)
n=mode (integer 0,1,2..)
L=length of patch (m)
W=width of patch (m)

In susceptibility analysis, the IC may be considered as a resonant system in very high frequency (Figure 9-32). The screen "**Tools→Patch Resonant Frequency**" computes the resonant frequencies according to the above formulation.

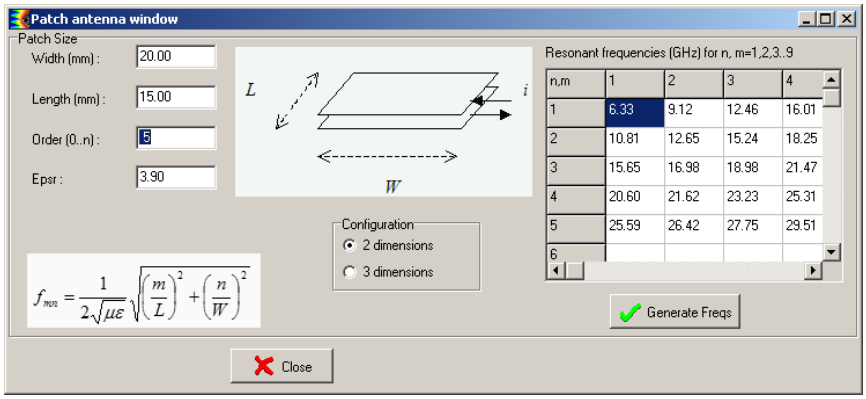


Figure 9-32 : Computation of the patch antenna frequency

9.1.41 Print Schema

Click on **File →Print Schema** to transfer the graphical contents of the screen to the printer. Alternatively,

you can make a copy of the window into the clipboard in order to import the screen into your favorite text editor by pressing <Alt>+<Print Screen>. In the text editor or in the graphic editor, simply click on "**Edit →Paste**" We recommend that you switch to monochrome mode first by invoking the function **File → Monochrome/color**. In that case the layout will be drawn in a white background color using gray levels and patterns.

9.1.42 Properties

The command "**File → Properties"** provides some information about the current technology, the percentage of memory used by the schematic diagram and its detailed contents (fig. 9-33). It gives also an access to some special options for schematic design and debug features.

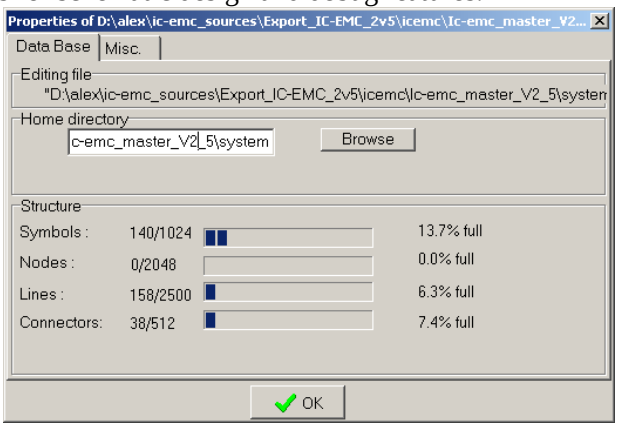


Figure 9-33 : File properties, including statistics about the number of symbols, nodes and lines

9.1.43 PWL Source Generator

The Piece-Wise-Linear source generator (**Tools → PWL Source Generator**) is a convenient way to build an arbitrary input waveform as a voltage source for simulation. A powerful mathematical set of routines enable to describe virtually any waveform and transform it into a series of (Time,Voltage) points. Predefined waveform descriptions are proposed in the upper menu, based on a reduced set of parameters that are listed on the right side. The user can manually edit the equation in order to obtain its own waveform. The output of this tool is a text file that is compatible with SPICE PWL source description. Voltage and current sources proposed by IC-EMC can be defined with a PWL description, the path of the text file must be specified.

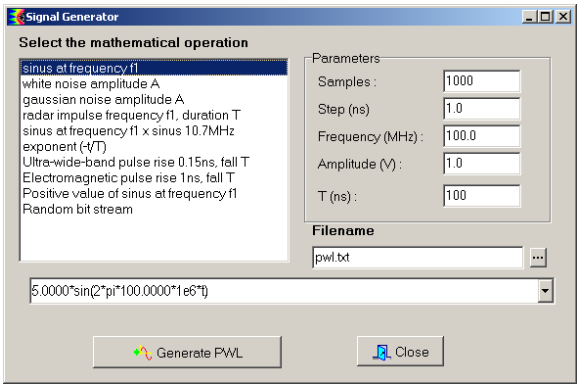


Figure 9-34 : PWL generator example

An example of output TXT file ("PWL.TXT" by default) is given below:

- PWL description for 1.0000*exp(-t*/0.15e-9)-exp(-t*/100.0000e-9)
  +(0.0NS 0.0000 1.0NS -0.9888 2.0NS -0.9802 3.0NS -0.9704 4.0NS -0.9608
  5.0NS -0.9512 6.0NS -0.9418 7.0NS -0.9324 8.0NS -0.9231
  +9.0NS -0.9139 10.0NS -0.9048 11.0NS -0.8958 12.0NS -0.8869 13.0NS -
  0.8781 14.0NS -0.8694 15.0NS -0.8607 16.0NS -0.8521
  ...

Number of samples and step of the PWL description are given by the fields “Samples” and “Step (ns)”.

9.1.43.1 Mathematical functions

Function	Description
Abs	Absolute value
Arcos	Invert cosine
Arcsin	Invert sinus
Arctan	Invert tangent
Abs	Absolute value
Avg	Average of the signal
Cos	Cosine
CosH	Hyperbolic Cosine
Exp	Exponent
Gauss	Gaussian noise; the parameter is the variance
Int	Integral
Logic	Random logic value between VDD and VSS, changed at period given as a parameter.
Norm	Normal distribution
Pi	3.1415927
P2	2*pi
Pos	Positive value of the signal
RMS	Root mean square
Sin	Sinus
SinH	Hyperbolic Sinus
Sqr	Square
Sqrt	Square root
White	White noise; the parameter is the amplitude
t	Time in seconds
Tan	Tangent
Vdd	Voltage supply; given in the technology file
x	Time in seconds

9.1.43.2 Function Examples

A user’s defined equation may be entered to create virtually any type of waveform. Examples are given below. The full list of functions is reported in table 9-3.

Function declaration	Function description
10.0*sin(2*pi*100e6*t)	100 MHz sinusoidal wave, 10 V amplitude
white(3.0000)	White noise, amplitude 3 V
gauss(1.0000)	Gaussian noise, amplitude 3 V
10*exp(-sqr((t-100e-9)/100e-9))*sin(2*pi*1^{e}9*t)	Radar pulse at 1 GHz, starting at 100 ns, 10 V amplitude
100*(exp(-t*/100.0e-9)-exp(-t*/0.15e-9))	Ultra-wide band pulse, 100 V amplitude (double exp)

Table 9-3 : examples of function declaration

Some basic impulse waveforms are proposed in the upper menu of the PWL generator, which gives the result shown in Fig. 9-35-right. The output of this tool is a text file that is compatible with SPICE PWL source description.

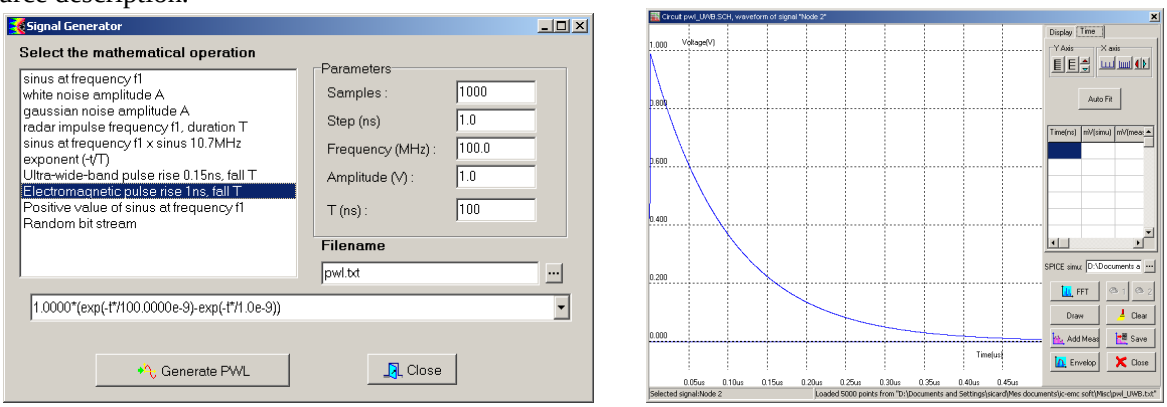


Figure 9-35 : Generating the PWL description of an electromagnetic pulse

The PWL source generator proposes also to generate a random bit stream (select 'Random bit stream' under Select the mathematical operation). No equations are defined, the user only provides characteristics of the stream (amplitude of low and high levels, and signal frequency) and an optional initial bit sequence e.g. 01101010. The length of the bit stream is arbitrary.

9.1.44 RFI control

The command **View → RFI Control** is used to open the susceptibility simulation configuration interface (see chapter 7 for more information about susceptibility simulation). This simulation requires the presence of a RFI source and a coupler in the IC-EMC schematic.

9.1.45 Rotate (or CTRL-R)

To apply a rotation to one part of the design, click "**Edit → Rotate".** Select one of the proposed action:

- Rotate right or 90°
- Rotate left or -90°

Then, delimit the area inside which the elements will be rotated.
To rotate one single symbol, simply place the cursor above the desired symbol and press CTRL+R.

9.1.46 S parameter analysis

The command "**EMC → S parameter**" gives access a specific screen for comparing measured and simulated S parameter. The simulation result file is the result of an AC simulation where one or more ports have been defined. The S parameters between each of these ports are computed at each frequency defined by the AC simulation. S parameter simulations are limited to 4 active ports and 4000 frequency points.
The simulation results are written in several .txt files associated to a given S parameter (for example S11_file_name.txt). The parameters of the simulation and the result file names are listed in a *.spc file. Figure 9-36 shows the screen "**S Parameter Analysis**". The simulation file is chosen in the field "Simulation Data Source", the list of simulated S parameters appears just above in the list "S parameter". Different values associated to S parameter can be selected in the list "Value":

- Magnitude in linear scale “Mag (linear)”
- Magnitude in dB “Mag (dB)”
- Real part of the magnitude “Mag (real)”
- Imaginary part of the magnitude “Mag (imaginary)”
- Phase in degree “Phase (degree)”
- Phase in radian “Phase (radian)”

Click on button “Add” to display the selected S parameter in the chosen format. The S parameter can be converted in terms of Z parameter by clicking in the checkbox “Z” in the “Conversion” field. X and Y axes can be set in linear or logarithmic format. S parameters can be displayed in a Cartesian graph (Amplitude vs. Frequency) or in a Smith chart.
Measurements can be imported in the field “S Parameter Measurement” in order to compare with simulation results. The S parameter data files are Touchstone file “*.snp”, where n is the number of port. See Appendix A for more information about Touchstone file format. Click on the button “Add Meas.” to display the measurement results and compare them to simulation results. Click on the button “Save” to export simulation results in a standard Touchstone file.
If you click directly on the screen, the corresponding coordinate appear on the screen. If the curves are displayed in a Cartesian graph, the coordinates indicates the frequency and the value of the point on which the user have clicked. If the curves are displayed in a Smith chart, the frequency, the amplitude in linear and the phase in degree of the closest point of the closest curves are returned.

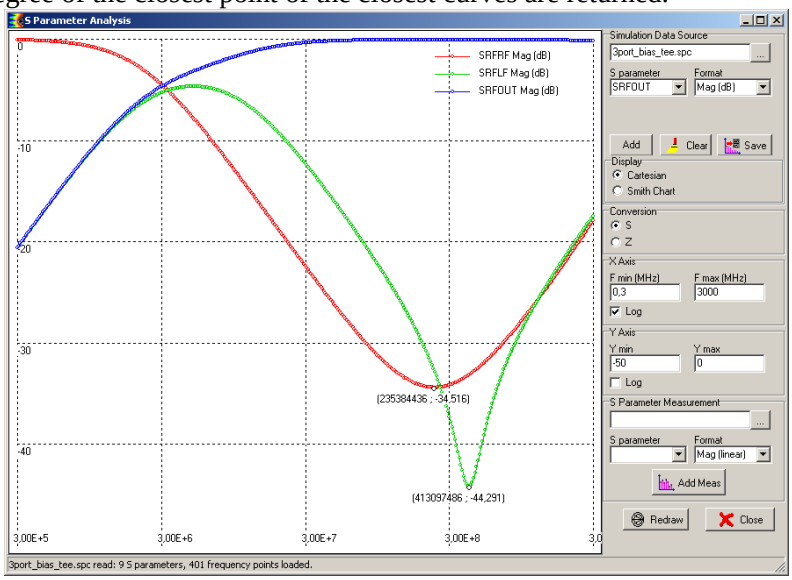
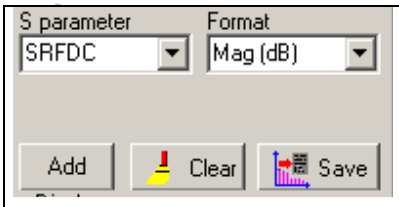
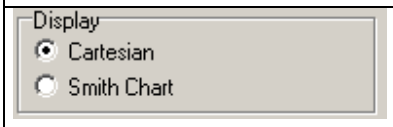
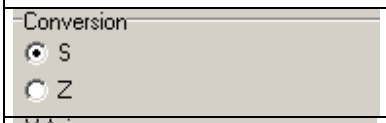
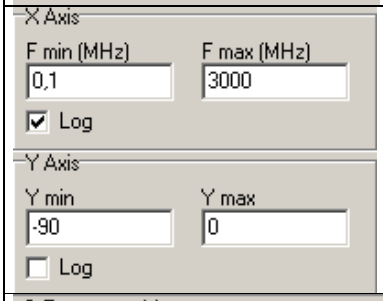
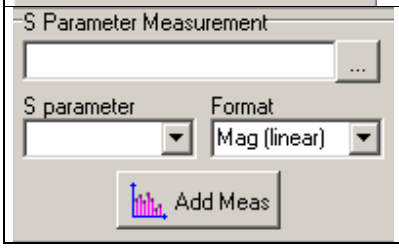


Figure 9-36 : S parameter analysis user’s interface (EMC_lib\3port_bias_tee.sch)

9.1.46.1 Control Buttons

Buttons	Description
Simulation Data Source bias_tee_150K_2GHz.spc ...	Import the S parameter simulation control file *.spc. If a schematic corresponding to a S parameter simulation is opened, the associated .spc file is opened.

	Add a simulated S parameter o nthe graph or clear completely the graph. Save all the S parameters in a Touchstone *.s*n*p file. If “Conversion” is set to S, the S parameters are saved in term of S parameter. It it set to Z, they are saved in term of Z parameters. The box “S parameter” lists all the S parameters between the N active ports defined in the schematic. The box “Format” lists the different format proposed by IC-EMC to display the S parameters: magnitude in linear or dB scale, real and imaginary part, phase in degree or radian.
	Display S parameters in a Cartesian graph or in a Smith chart. Suppose that several curves are displayed in a Cartesian graph. If you want to display curves in a Smith chart, click on the box “Smith Chart”, the previous curves are cleared. Then click on the button “Add” to display new curves in a Smith chart.
	Simulated and measured S parameters displayed on the screen are automatically converted in S or Z parameters when the corresponding box is selected.
	Axis settings. Each time a new curve is added, the axis settings are lost and replaced by default axis settings. The default settings are computed to display all the curves.
	Display S parameter measurements. Format of measurement is Touchstone file *.snp. Choose the measurement file, then choose the S parameter to display and its format and click “Add Meas” to display the measurement.

9.1.47 S parameter de-embedding

The command "**Tools → S Parameter Deembedding**" gives access a specific screen for deembedding a S11 parameter measurement. Deembedding a S11 parameter measurement means removing the influence of parasitic attachments (coaxial cables, microstrip lines …) used to connect the device under test input to the calibration plane of a vector network analyzer. See Appendix D for more information about S parameter deembedding. The raw S11 measurement can be provided by a file in .s50 or Touchstone .s1p format (see Appendix A for more information about these formats). Data in this file can be in various formats:

- S or Z parameter
- Real and imaginary parts
- Amplitude and phase

The maximum number of frequency is limited to 4000 points. The deembedding process considers two cases:

- the DUT is connected to the calibration plane of the VNA by a perfectly matched transmission line. Only the delay and thus the phase introduced by the line are compensated by the deembedding process.

- the DUT is connected to the calibration plane of the VNA by an unmatched 2-port device. A touchstone file .s2p must be provided by the user to characterize this device. The .s2p file of the 2-port device must contain the same number of frequency points than the raw S11 measurement file to perform the deembedding. If the frequencies in both files are not identical, validity of deembedding results can not be ensured.

The interface proposes a screen used to display the S11 raw measurement file and the deembedding results, as shown on figure 9-37. Data are displayed in impedance amplitude versus frequency. Deembedding results, i.e. the S11 parameter of the load after removing the parasitic attachments, can be saved in an output file in three different formats: .z, .s50 or .s1p. The two first formats are dedicated to display the results in the tool "Impedance vs. Frequency", while the last format is dedicated to display the results in the tool "S parameters vs. Frequency". The result can be displayed in these screens as measurements.

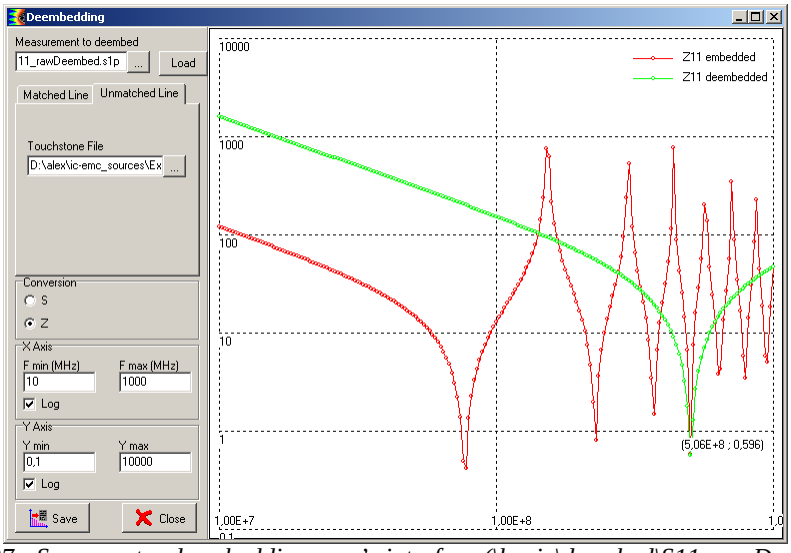
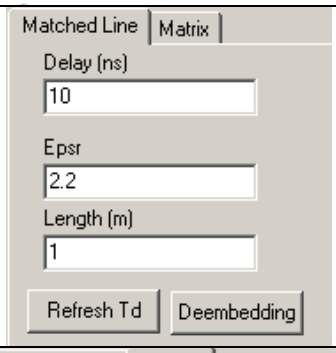
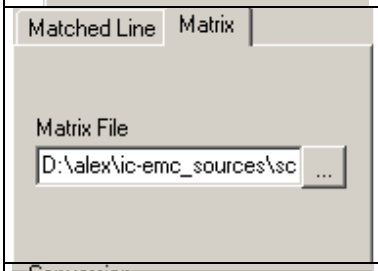
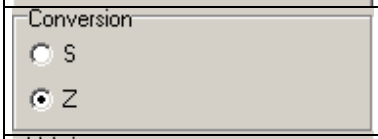
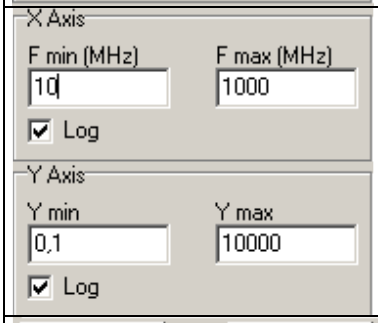


Figure 9-37 : S parameter deembedding user's interface (\basic\deembed\S11_rawDeembed.s1p)

9.1.47.1 Control Buttons

Buttons	Description
Measurement to deembed D:\alex\ic-emc_sourc ... Load	Import the S11 raw measurement file, that consists of the measurement of the device under test connected to the VNA through a matched or unmatched connection. The file could be in .s50 or .s1p format. Select the file and click on the button "Load" to load the raw measurement file and display the measurement in an impedance vs. frequency chart.

	The connection between the load and the VNA is a matched transmission line (Tab “Matched Line”). Specify the delay introduced by this line: type directly the delay in ns, or type the length and the relative dielectric constant of the line and click on the button “Refresh Td”. Once the delay has been specified, click on the button “Deembedding”. The effect of the connection is removed and the impedance profile of the extracted load is traced.
	The connection between the load and the VNA is an unmatched 2-port transmission line (Tab “Matrix”). Specify the path of the Touchstone file *.s2p which characterizes the unmatched line. Once this file has been identified, the deembedding is automatically performed. The effect of the connection is removed and the impedance profile of the extracted load is traced.
	The raw measurement and the deembeding results displayed on the screen are automatically converted in S or Z parameters when the corresponding box is selected.
	Axis settings. Each time a new curve is added, the axis settings are lost and replaced by default axis settings. The default settings are computed to display all the curves.
	Click on the button “Save” to export the deembedding results in either a .z, .s50 or .s1p file. Click “Close” to close the interface.

9.1.48 Save (CTRL+S), Save As

Click “**File → Save”** to save the schematic diagram with its current name. The default name is " EXAMPLE.SCH ". In the case of "Save As…", a new window appears, into which you are to enter the design name. Use the keyboard and type the desired file name. Press " Save ". Your design is now registered within the **.SCH** appendix.

9.1.49 Select Technology

Click on “**File → Select Technology”**. The list of available processes appears. The initial design rule file is "default.tec". Various technologies are available from 1.2µm down to 90nm. Click on the rule file name and the software reconfigures itself in order to adapt to the new process. See Appendix B for more information on the format of the TEC file.

9.1.50 Signal analysis

The command **EMC → Signal Analysis** opens a special window to extract statistical information about amplitude and timing characteristic of a signal. The tool is also available from "**EMC → Voltage vs. Time**" interface. The tool loads the transient simulation results contained in a .txt file. If a schematic is opened and have been simulated, the simulation results in *.txt file are automatically loaded (whatever the simulation type!). The simulation result file can also be imported, with the field 'Simulation Data Source'.
The tool offers two types of signal analysis:

- tracking analysis (Time domain category): the transient evolution of the signal (i.e. its amplitude) or one of its timing characteristics (Fig. 9-38)
- statistical analysis (PDF category): the statistical distribution of the signal amplitude or one of its timing characteristics, given in term of probability density function (PDF) (Fig. 9-39). Statistical properties such as minimum, maximum, mean values, peak-to-peak amplitude and standard deviation are also given under the graph.

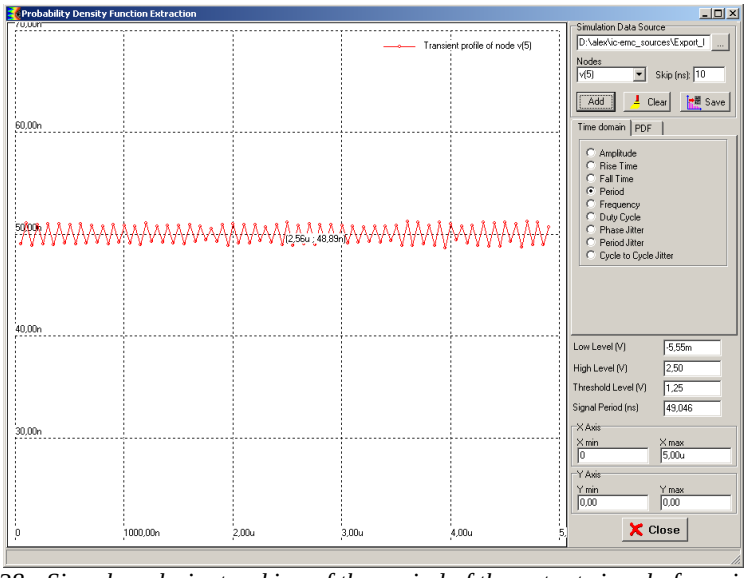


Figure 9-38 : Signal analysis: tracking of the period of the output signal of a noisy inverter (\misc\noisy_inverter.sch)

The following timing properties can be extracted:

- rise and fall time: the time required for the signal to go from 10% to 90% of the maximum amplitude (defined by High Level – Low Level fields defined by the user)
- period and frequency of the signal: the period is measured between two adjacent instants when the signal crosses the Threshold limit defined by the user (by default, threshold = 0.5×(High Level + Low Level). The frequency is equal to the invert of the period
- Duty Cycle: the period ratio during which the signal exceeds the Threshold level

Phase, Period and Cycle-to-cycle jitter: three different definitions of the jitter [9-3] [9-4]. The phase, edge, timing or absolute jitter, or time interval error is the deviation in the transition of the signal from its ideal position (the ideal position is defined by an ideal clock which starts with the characterized signal and with a period defined by the field 'Signal Period (ns)'). The phase jitter characterizes each signal period. The

period jitter is related to the fact that the phase jitter tends to diverge with measurement time due to jitter accumulation in real oscillators, so that phase jitter is not the best figure of merit for jitter characterization. Period jitter is the deviation of the signal period with respect to the ideal clock period. Period jitter originates from two timing errors on both rising edge of two adjacent periods. Period jitter is the first jitter difference. Cycle-to-cycle jitter characterizes the variation of signal period between two adjacent periods. It describes the short-term dynamics of the period.

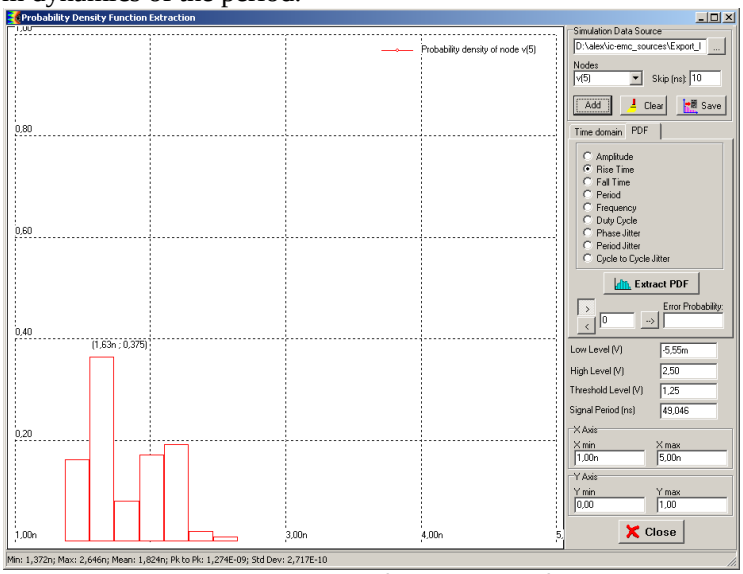


Figure 9-39 : Signal analysis: statistical distribution of the rise time of the output signal of a noisy inverter, given in term of probability density function (PDF) (\misc\noisy_inverter.sch)

9.1.51 Spectrogram

The command "**Tools → Spectrogram**" gives access to the display of the energy (using a palette of colors) versus time, where the Y axis is the frequency. The spectrogram is obtained by computing several FFT and shifting the FFT window until the whole signal is covered, as explained in figure 9-40. The FFT is applied iteratively on a reduced number of points, and then shifted and X and Y axis may be modified using the icons situated on the top-left corner of the screen.
The command "Play Sound" converts the signal into a WAV sound and executes it on the windows mediaplayer.

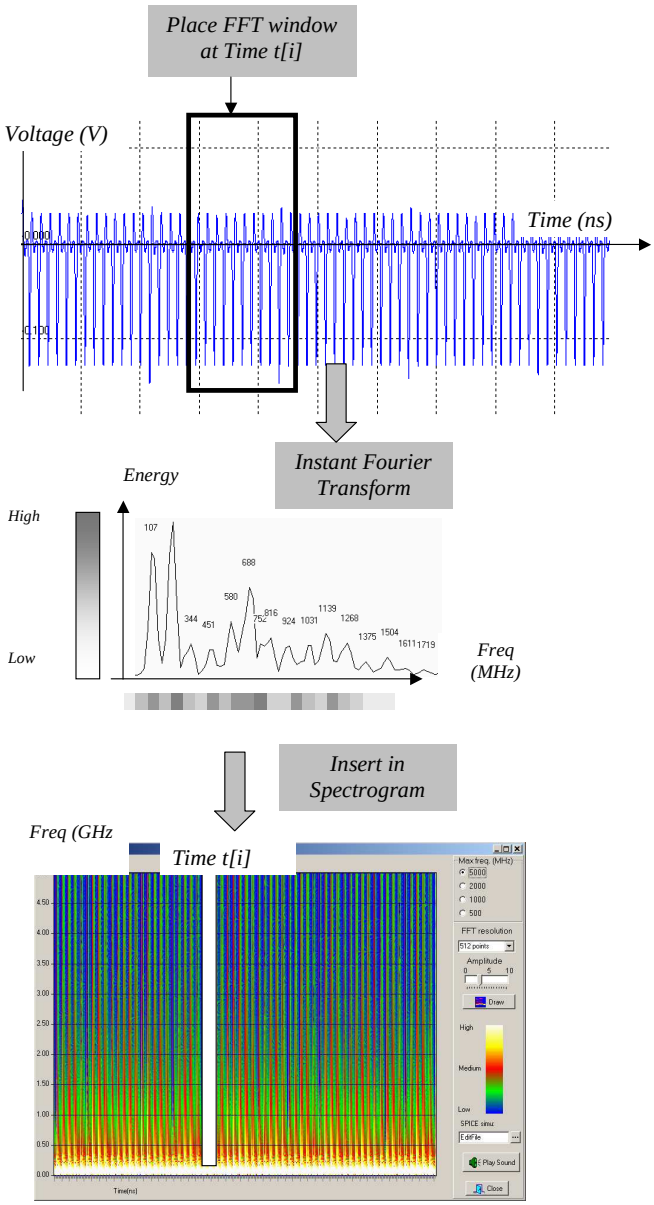


Figure 9-40 : Spectrogram principles

9.1.52 Susceptibility dBm vs. Frequency

The command "**EMC → Susceptibility dBm vs. Frequency**" gives access to a screen dedicated to susceptibility simulation control and susceptibility level extraction. Figure 9-41 presents the user interface of this tool, composed of two screens:

- the left part is dedicated to the control of the susceptibility simulation (parameters of the RFI source, definition of the susceptibility criterion, parameters of susceptibility threshold extraction). This screen proposes 2 tabs corresponding to the two simulation modes: manual and automatic. The difference between both modes is linked to the frequency sweep.

- the right part plots either the transient profile of the signal used as susceptibility criterion, or the extracted susceptibility threshold, given in term of dBm vs. frequency.

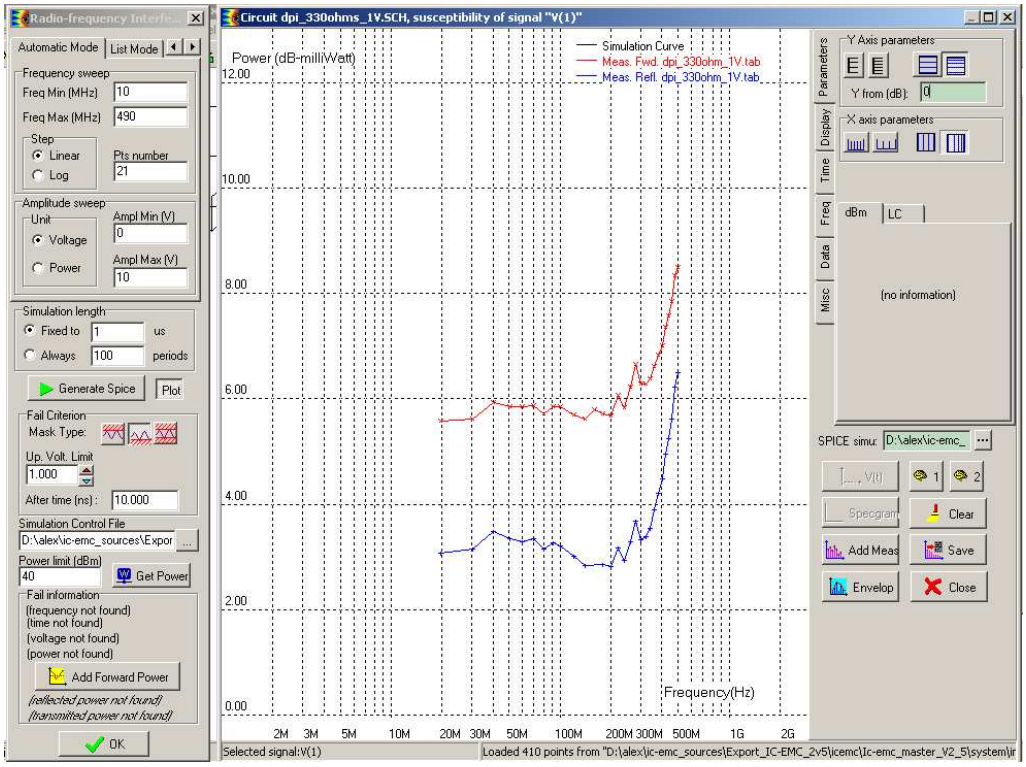
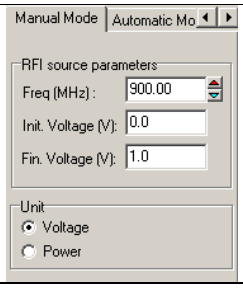
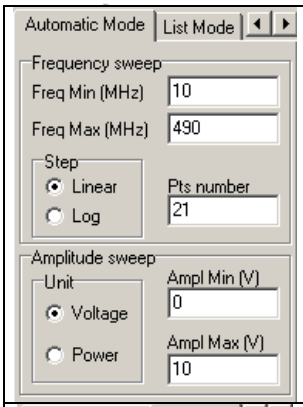
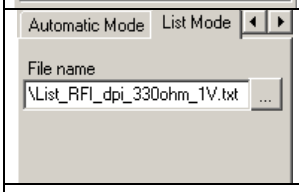
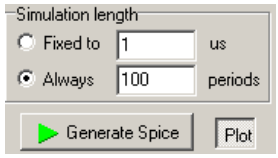
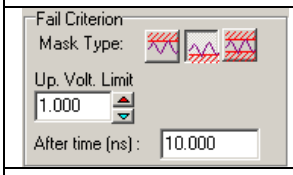
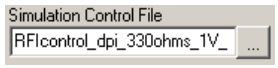
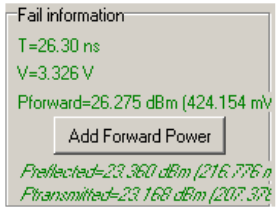


Figure 9-41 : The immunity simulation screen

First, configure the RFI and the SPICE simulation. Then generate the SPICE netlist and launch the SPICE transient simulation. At the end of the simulation, configure the susceptibility criterion and extract the susceptibility threshold.

9.1.52.1 Control Buttons

Buttons	Description
	Control of the RFI source in Manual mode. Set the frequency of the RFI source, the start and stop amplitude of the RFI source. The amplitude can be defined in term of voltage (V) or power (dBm) depending on the option “Unit”. The voltage defines the amplitude of the voltage source included in the RFI source, so that it does not define the output voltage of the RFI source. The power defines the maximum available of the RFI source. It represents the power provided by the source to a matched load.

	Control of the RFI source in Automatic mode. This screen is split in two parts: Frequency sweep and Amplitude Sweep. First, set the frequency range of the RFI source: the start and stop frequency and the number of frequency points. The frequency sweep is linear. Then, set the the start and stop amplitude of the RFI source. The amplitude can be defined in term of voltage (V) or power (dBm) depending on the option “Unit”. The voltage defines the amplitude of the voltage source included in the RFI source, so that it does not define the output voltage of the RFI source. The power defines the maximum available of the RFI source. It represents the power provided by the source to a matched load.
	Control of the RFI source in List mode. All the configuration of RFI source, the transient simulation duration and the susceptibility voltage criterion for the different RFI frequencies are defined in a tabulated text file. See immunity\dpi330ohm \List_RFI_dpi_330ohm_1V.txt as example.
	Configuration of the SPICE transient simulation. The simulation length is set in term of time (case “Fixed to”) or RFI periods (case “Always”). This second option is adapted in automatic simulation mode when the simulation covers a large frequency range. If a fixed simulation duration is used for every frequency, this duration can be too short for low frequencies and too large for high frequencies. Click on the button “Generate Spice” to build the SPICE netlist of the susceptibility simulation.
	Configuration of the failure criterion. In this version, only a voltage level criterion is proposed. Type the voltage limit in the field “Voltage” and click on the three Mask Type buttons to define the polarity of the criterion. The definition of the criterion is required only after the SPICE simulation in order to extract the susceptibility threshold.
	This field appears only in automatic mode to import simulation result files. WinSPICE exports transient simulation results in .txt file for each frequency of the RFI. In automatic mode, a large number of .txt files are generated. A simulation control file .ctl is used to locate all the simulation result .txt files.
	The field “Power limit (dBm)” set a default power value if the failure criterion is not detected during a transient simulation. If the simulation is compared to a susceptibility measurement, this limit should be equal to the power limit in measurement, due to the limitation of the power amplifier. Click on the button “Get Power” to extract the susceptibility threshold. On the right screen, the transient profile is plotted to show the time when the failure is detected.
	Information of susceptibility threshold extraction process is indicated here. In manual mode, the time, the voltage, the forward, reflected and transmitted power when the failure appears is written. In automatic mode, the same information is written but only for the last frequency point. Click on the button “Add Forward Power” to add a new point to the susceptibility threshold in Manual mode, or to plot the extracted susceptibility threshold in Automatic mode. Click on the button “Save” on the right screen to save the extracted forward power. Click on the button “Add Meas.” to add a measurement. Measurements of susceptibility threshold are imported in .tab file (see Appendix A).

9.1.53 Symbol Library

The palette symbol library contains basic electrical symbols, sources, probes and switches. The palette is visible by default. It can be closed by the user. The command **View → Symbol library** or the icon  makes the palette visible. The symbol library is reported in the reference manual. Additional symbols may be found in the "ieee" sub- directory, accessible through the command **Insert →User Symbol**.

Element	Description	Symbol name
Resistor	Resistor between two nodes	res.sym
Capacitor	Capacitor between two nodes	capa.sym
Inductance	Inductance between two nodes. With the "Assign [x;y] coordinates" property, "radiating inductance" can be defined for H field simulation (Near field scan simulation).	self.sym
OpAmp	Operational amplifier, with programmable gain	aop.sym
RLC	R,L,C using a "pi" model , which can be computed from 2d description of the interconnect	rlc.sym
Mutual Coupling	Defines the mutual coupling between two inductances.	mutual.sym
Radiated interconnect	Interconnect defined by a lumped pi-RLC cell. (X;Y;Z) coordinates, width and length are attributed to the interconnect. The property "Allow near field scan computation" ensures the simulation of E and H field (Near field scan simulation).	Interco.sym
T-Line	Transmission line, with user-accessible T0, Z0, or delay parameters	tline.sym
Coupler	Bidirectional coupler, required to extract forward and reflected voltage or power (on 50 Ω load). This element must be inserted during susceptibility simulation.	Coupler.sym
V-source	Voltage source	vsource.sym
I-source	Current source	isource.sym
RFI-source	Radio Frequency interference source, used for immunity simulations. Includes a programmable frequency generator with linearly increased amplitude vs time.). This element must be inserted during susceptibility simulation.	rfi.sym
Ground	Ground connection equal to 0.0V	vss.sym
Supply	Supply source with DC value equal to the default supply value that is found in the technology configuration file "default.tec"	vdd.sym
Voltage controlled Vsource	Voltage controlled voltage source. This source can model an ideal amplifier with a constant gain.	vcvs.sym
Non linear element	Non linear voltage or current source, called B element in WinSPICE syntax.	Belement.sym
V-probe	Voltage probe (voltage measured according to the potential 0)	probe.sym
V diff-probe	Differential voltage probe (voltage difference measured between two nodes)	probeVdiff.sym
I-probe	Current probe (serial probe with orientation marked by + symbol).	probeI.sym
Z-probe	Used to generate an AC sinusoidal source to extract the impedance vs. frequency	probez.sym
S-probe	Used to declare port for S parameter analysis.	Sport.sym
IC	Initial conditions. Used to fix the start value of a node (V).	ic.sym

nMOS	N-channel MOS device. Uses “spice.lib” where the MOS parameters can be described and modified.	nmos.sym
pMOS	P-channel MOS device. Uses “spice.lib” where the MOS parameters can be described and modified.	pmos.sym
Inverter	Inverter that combines one nMOS as pull down and one pMOS as pull-up	inv.sym
I/O	Input/output symbol. Used to specify the name of the I/O of a sub-circuit, during the sub-circuit definition process	io.sym
Box	Size-programmable dotted box	box.sym
Information	Information symbol with fields such as: author, date, file, project, or comments	info.sym
Arrow	Define an electrical connections between wires connected to arrow with the same name (the name of the arrow is arbitrary).	Arrow.sym

Table 9-4 : Description of each symbol of the palette

9.1.54 Symbol Color

The command “**Edit → Symbol Color**” is useful to change the color of a group of symbols included in a given area. The same result is obtained by successively clicking inside each symbol and altering the color parameter. It is recommended to assign different colors to different parts of the schematic diagram.
A proposed color assignment is as follows:

- IC-related symbols are in yellow
- Package-related symbols are in red
- Probe-related symbols are in blue
- External symbols are in green (default color)

9.1.55 Text

Use this icon  (or **Edit → Text**) to define a text to one box or location in the design. That text sets simulation commands, illustrates the layout and should be used as much as possible for each significant node such as inputs and outputs. To add some text to a particular place, proceed as follows:

❶ Click on the icon
❷ Set the text location with the mouse. A dialog box appears
❸ Enter the text in front of “Text:” and press “Ok”. The text is set in the drawing

A text can be modified as follows: click on the icon, click inside the existing text. The old text appears. Modify it and click on “Ok”. Text is added for information only. It has no impact on simulation.
If text is added for information only, it has no impact on simulation. Text is useful to add comments on the schematic diagram, add more information or specific I/Os or nodes.
Note that text starting with “.” is usually considered as a simulation command. For example: “.TRAN 0.1NS 100NS” is a text that is also considered as a SPICE control to configure the transient simulation.

Keyword	Used for	Example	Parameters
.TRAN	transient simulation	.TRAN 0.1NS 100NS	Step, duration
.DC	dc simulation	.DC Vin 0 5 0.1	Voltage, start voltage, stop voltage, voltage step

.AC	AC simulation	.AC DEC 10 1MEG 1G	DEC = decade, points per decade (10), start freq (1 MHz), stop freq (1 GHz)
.IBIS	Load IBIS file	.ibis cesame_v14.ibs	Name of the Ibis file
.LIB	Load SPICE library	.lib cesame.lib	Name of the text file that includes the component models. The default library is 'spice.lib'
KA	Inductance coupling	K2 Ltem2 Lvdd 0.002	Coupling between inductor 1, inductor 2 and coupling coefficient (between 0 and 1)
.OPT	WinSpice option	.OPT RELTOL=1e-6	.OPT RELTOL=1e-6
.SCAN	Scan configuration	.scan 1e-3 10e6 3.5e-3 2.1e-3	Scan step (1e-3), scan frequency (10 MHz), scan altitude (3.5 mm) and lead altitude (2.1 mm)
.PLOT	Plotting signals	.plot v(1) .plot –i(vsource)	Lists the voltage or current to appear in the Spice simulation
.FAIL	Immunity threshold	.fail 1.0V .fail < 0.5V	Fixes the voltage threshold used in immunity simulation. The signs '>' or '<' indicate a rise or fall edge detection.
.VDD	Supply Voltage	.vdd 3.3V	Fixes the general supply voltage to the desired value. Otherwise, the default VDD value of the technology file (default.tec) is used.
.SCRIPT	Add a script from a text file	.script iteration.txt	Replace the 'run' section in the Spice netlist by the text contained in the user's defined text.
.TEMP	Define temperature	.temp 85	Defines the simulation temperature. By default, 25℃ is used.

9.1.56 Undo (or CTRL+Z)

The Undo command ("**Edit → Undo"**) is useful to cancel the last editing command. It is possible to undo the commands Cut, Paste, Copy, Move, Stretch, & Edit.

9.1.57 Unselect All (Escape Key)

Use the command "**View → Unselect All"** to cancel undesired commands, or to redraw the complete schematic diagram.

9.1.58 View All (CTRL+A)

Click "**View → View All"** to fit the screen with all the graphical elements currently on display.

9.1.59 View Same

Click "**View → View same"** to draw again the schematic diagram without changing the scale. This function is used to refresh the screen.

9.1.60 Voltage Versus Time

The command "**EMC → Voltage vs. Time**" gives access to the time-domain waveform of the signal under investigation (Fig. 9-42). The X axis (time) and Y axis (volt) may be modified using the icons situated on the top-left corner of the screen. Click auto-fit to adjust the scale to include all the waveform, or define your own boundaries to zoom at a particular place. Click "FFT" to display the frequency-domain aspect of the wave, and "Spectrogram" to display the FFT in time domain (See "Spectrogram" for more information). Click the button "Signal Analysis" to display the timing evolution or statistical properties of a transient signam.

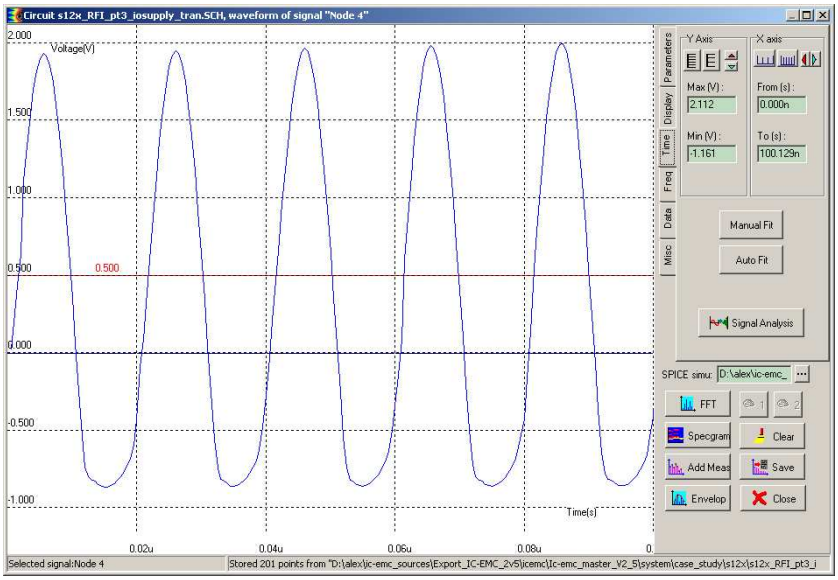


Figure 9-42 :Time-domain aspect of the signal under investigations (case_study\s12x\s12x_RFI_pt3_iosupply_tran.sch)

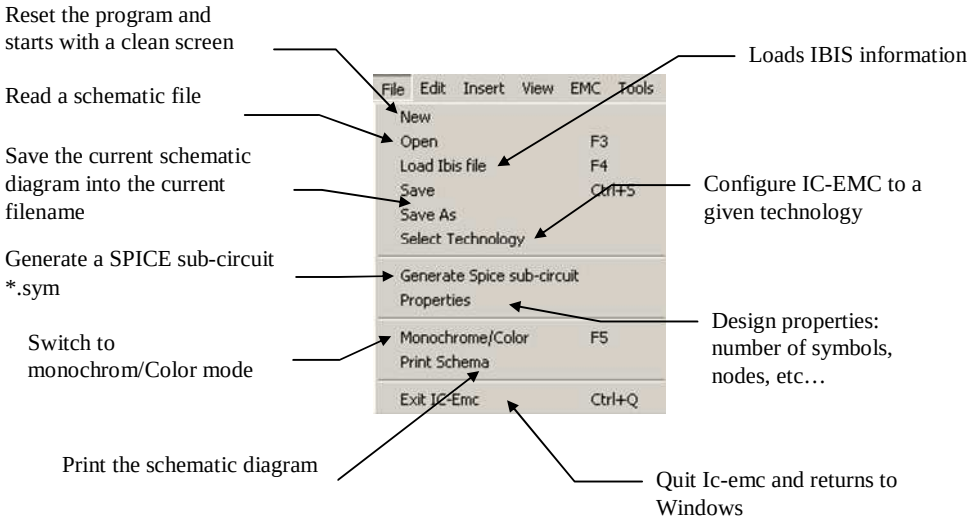
9.1.61 Zoom In & Out

The above icons perform Zoom In and Zoom Out. When zooming in, the area determined by the mouse will be enlarged to fit the display window. When zooming out, the area determined by the mouse will contain the display window.

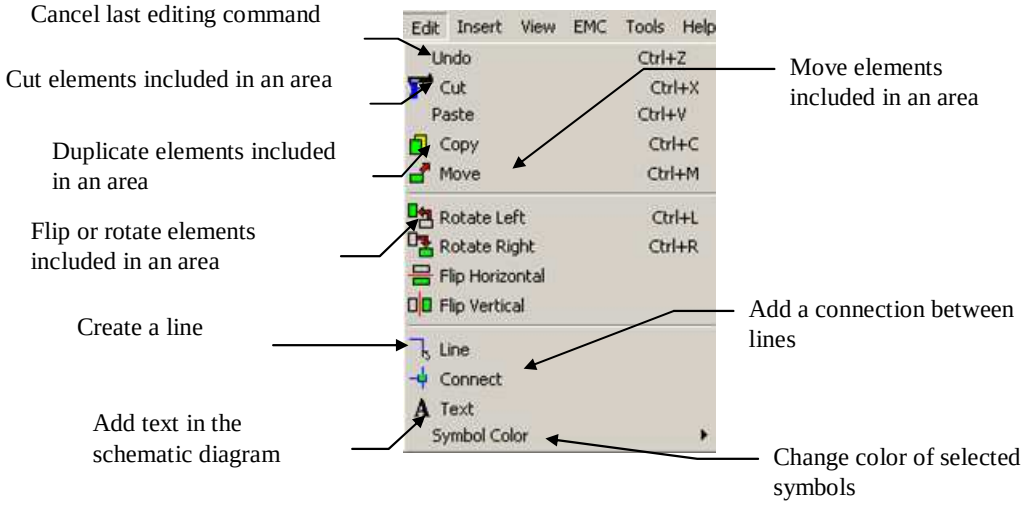
- If you click once, a zoom is performed at the desired location.
- Press Ctrl+A for « View All », and Ctrl+o for zoom out.

9.2 Quick Reference Sheet

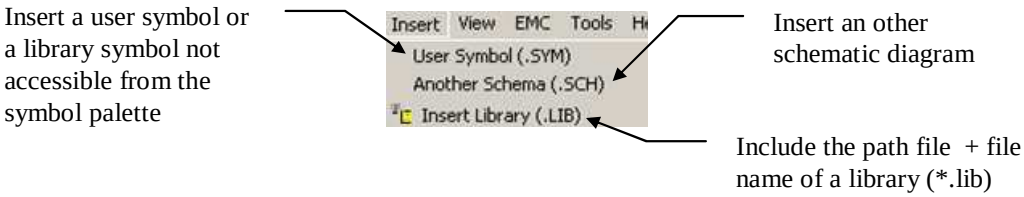
9.2.1 File Menu



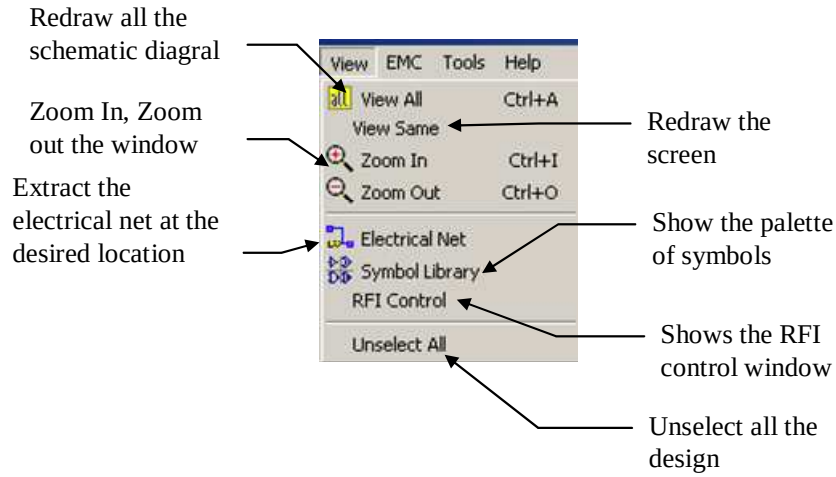
9.2.2 Edit Menu



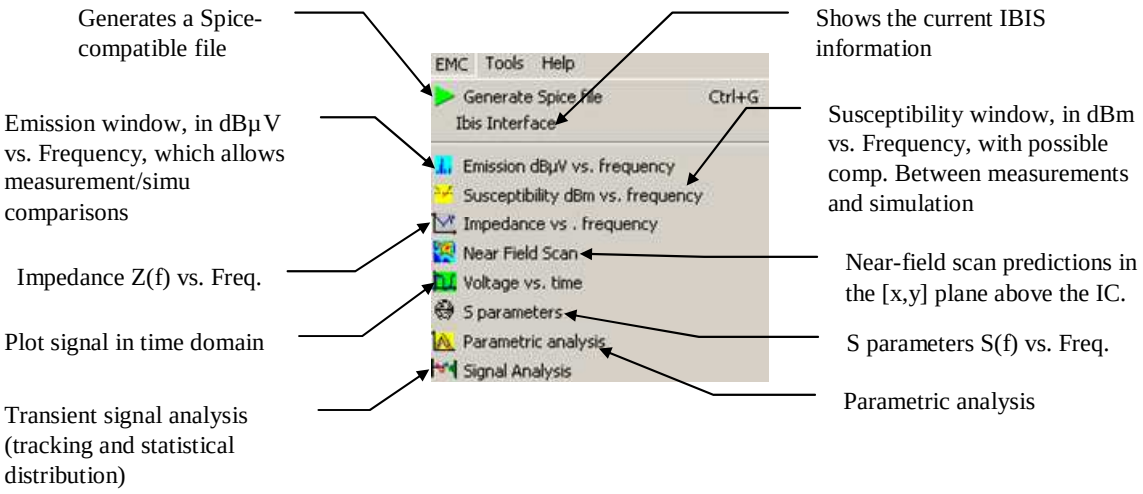
9.2.3 Insert Menu



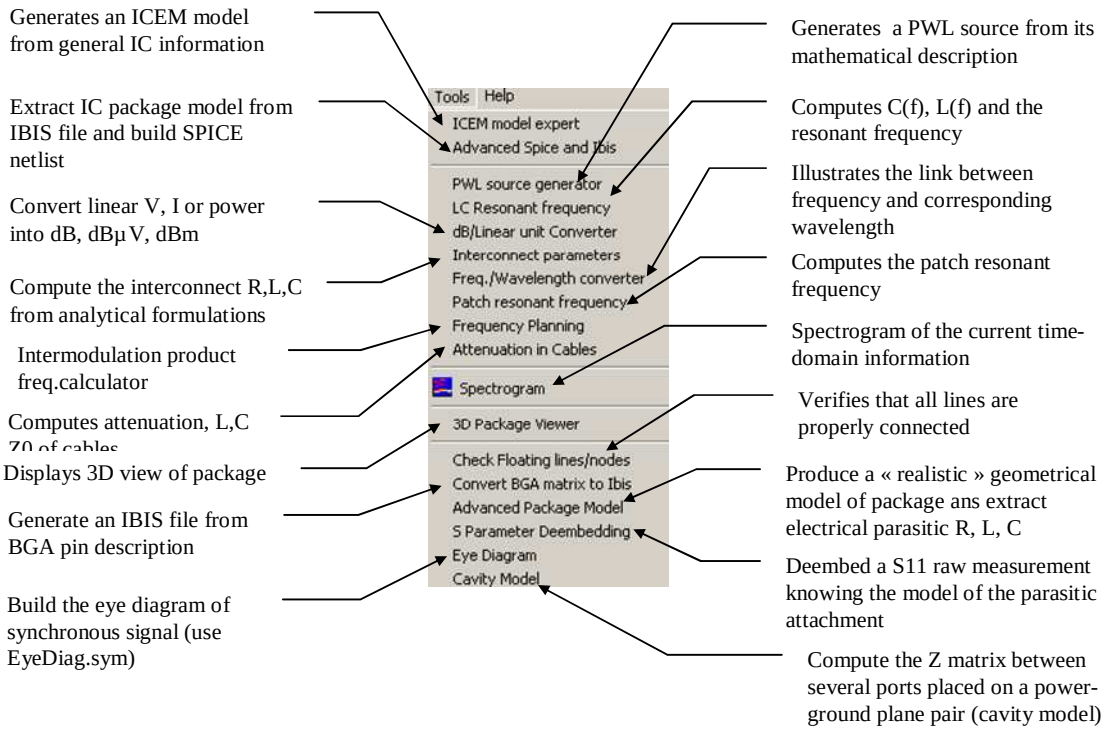
9.2.4 View Menu



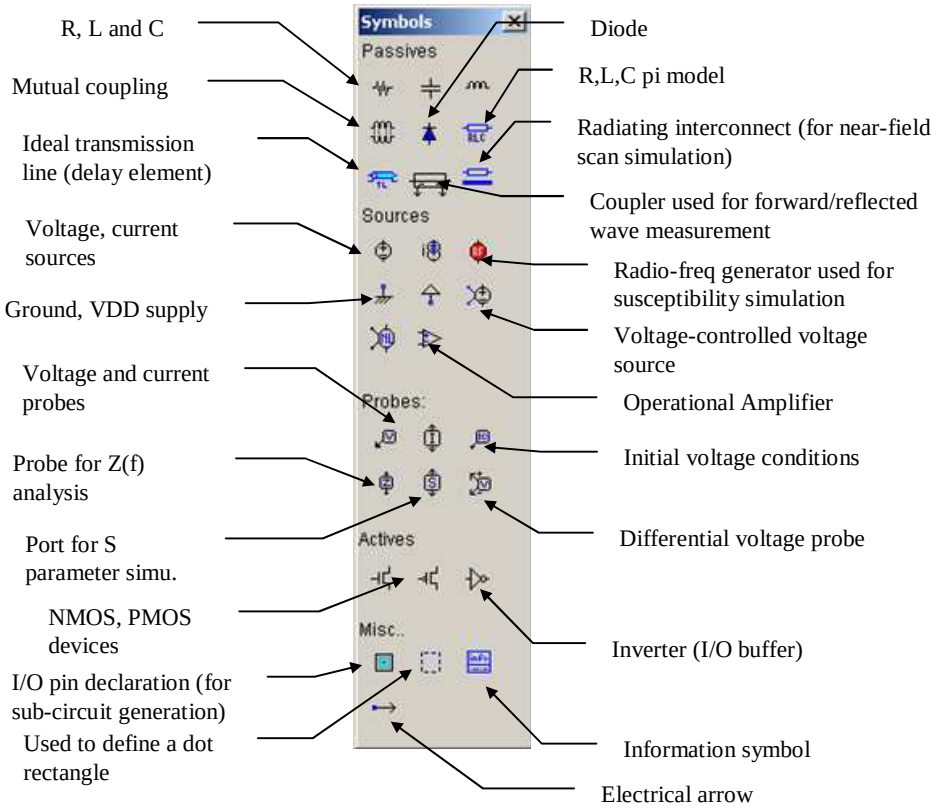
9.2.5 EMC Menu



9.2.6 Tools Menu



9.2.7 Symbol Palette



9.3 References

[9-1] M. Xu and T. H. Hubing, “Estimating the power bus impedance of printed circuit boards with embedded capacitance,” IEEE Transactions on Advanced Packaging, vol. 25, no. 3, pp. 424–432, Aug. 2002.

[9-2] M. Swaminathan, A. Ege Engin, “Power Integrity Modeling and Design for Semiconductors and Systems”, Prentice Hall Modern Semiconductor Design Series, Prentice Hall Signal Integrity Series, ISBN 978-0-13-615206-4, 2007

[9-3] T. Xanthopoulos, “Clocking in Modern VLSI Systems”, Springer, 2009, ISBN 978-1-4419-0260-3

[9-4] F. Herzel, B. Razavi, ” A Study of Oscillator Jitter Due to Supply and Substrate Noise”, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 46, NO. 1, JANUARY 1999

10 Appendix A: interface formats

10.1 ADV Frequency File Format

The ADV format corresponds to raw data generated by the spectrum analyzer Advantest 3131 (1 MHz – 3 GHz). The text file format is: frequency (Hz), first column, followed by spectrum energy (dBµV).

```
"1010000","-7,6"
"1015000","-7,5"
"1020000","-7,0"
"1025000","-7,6"
"1030000","-7,1"
"1035000","-7,5"
"1040000","-7,0"
"1045000","-7,5"
…
```

10.2 TAB File Format

The TAB file format is generated by several equipments, and corresponds to a text document, organized with the frequency (Hz) in the first column, followed by spectrum energy (dBµV), followed by position. The heading of the file is made of three comment lines. This is the most common exchange file for emission and susceptibility measurement. This file can be easily produced from measurement files generated by measurement equipment.

```
Frequency (Hz)  dBuV
10E6                  2.11656
10.05E6         -1.02154
10.1E6          -4.87756
…
```

10.3 Z Format

The Z file is similar to the .tab file, except that it is dedicated to import/export impedance measurement. This file consists of the frequency followed by the module of the impedance. The three first lines of the heading are ignored.

```
CAPA  Impedance
100pF A5 impedance vs frequency
Freq(Hz) Z(f)
45000000  25.96613733
57443750  15.90372125
69887500  10.70620745
82331250  7.724689023
94775000  5.852317536
…
```

10.4 S50 and S Formats

These 2 files are dedicated to the plot of measured reflected coefficient S11 (for .S50 file) or input

impedance Z11 or Zin (for .S file) in a Z11 format. They present 3 columns: the frequency, the real part of S11, and the imaginary part of S11. IC-EMC computes the module of the input impedance using the following correspondence.
For ".s" format, the formulation of the impedance is immediate:

$$|Z_{in}| = \sqrt{R^2 + X^2}$$

where R and X are the real and imaginary part of the input impedance Zin

For ".s50" format, the formulation is more complicated as it includes the impedance Z_0, fixed to 50 Ω. We note R the real part of s11 Real(s11), and X the imaginary par Im(s11): $S_{11} = R + jX$.

$$Z_{in}(real) = Z_0\left(\frac{1-R^2-X^2}{(1-R)^2+X^2}\right)$$

$$Z_{in}(imag) = Z_0\left(j\frac{2X}{(1-R)^2+X^2}\right)$$

$$|Z_{in}| = \sqrt{Zin(real)^2 + Zin(imag)^2}$$

Below is an example of "s50" [s] measurement file.

```
PCB Board
Mesures S11(f)
Freq (Hz) Real(s11) Im(s11)
1000000 0.882568359     -0.468902588
1004326.68      0.881835938     -0.470703125
1008672.081     0.880554199     -0.472717285
1013036.282     0.87979126      -0.474334717
1017419.366     0.878875732     -0.476348877
1021821.414     0.877929688     -0.477966309
…
```

10.5 Touchstone file – S1P and S2P

Touchstone files *.sNp are standard ASCII text file used to exchange measurement done with vector network analyzer on an N-port device, such as S, Z, Y… parameters or noise measurement [12-1]. IC-EMC can import and export only .s1p and .s2p files associated to one and two port device characterization.
In order to identify the type and the format of data exported by the Touchstone file, the heading of the file includes an option line which starts by a '#' symbol. Lines which begin by a '!' are comment lines, the other are associated to data. For s1p and s2p files, all the lines start with the frequency followed by the data at this particular frequency. The general format of the option line is:

<frequency unit> <parameter> <format> R <n>

- Frequency unit: specifies the frequency unit. GHz, MHz, KHz, Hz, the default value is GHz.
- Parameter: specifies the type of network parameter data contained in the file. S for scattering parameters, Z for impedance parameters, Y for admittance parameters…
- Format: specifies the format of the network parameter data contained in the file: MA for

magnitude in linear + angle, DB for magnitude in dB + angle, RI for real + imaginary. Angles are always given in degree.

- R n: specifies the reference resistance in ohms. By default, the resistance n is 50 ohms.

The following paragraph presents an example of Touchstone file for a 2 port device S parameter characterization.

```
! FILE NAME
! DATE 04/16/2005  11:30
! CORRECTED   DATA
# GHz    S       MA      R    50.00
!   FREQ       S11M          S11A     S21M          S21A      S12M
S12A      S22M         S22A
 0.040000000 1.005455E+00   -4.544 1.851869E-03 -125.819 3.100761E-03
92.047 9.720316E-01  -48.382
 0.046225000 1.004641E+00   -5.303 9.987922E-04  150.437 1.392118E-03 -
129.477 9.695778E-01  -84.433
 0.052450000 1.000527E+00   -6.231 3.931841E-04 -114.647 4.805698E-04 -
157.052 9.653241E-01 -120.483
```

IC-EMC imports .s1p file in the “Impedance vs. frequency” interface, and imports/exports .s1p/.s2p files in “S parameter vs frequency” and “S parameter deembedding” “interfaces. We transform Magnitude/Angle values for [S] parameters into impedance using the following equations:

$$R = S11M\cos(s11A)$$

$$X = S11M\sin(s11A)$$

$$S11 = R + jX$$

$$Zin(real) = Z_0\left(\frac{1-R^2-X^2}{(1-R)^2+X^2}\right)$$

$$Zin(imag) = Z_0\left(j\frac{2X}{(1-R)^2+X^2}\right)$$

$$|Zin| = \sqrt{Zin(real)^2 + Zin(imag)^2}$$

10.6 XML Near-field Scan Standard implementation in IC-EMC

Near-field scan measurements and simulations generate a large amount of data. The format of the data is closely linked to the supplier of the acquisition or simulation software, rendering extremely difficult its exchange between suppliers, customers, EDA tool vendors, academics, etc. The XML format proposed in [12-2] describes how a common exchange format for near-field scan data has been developed. The format caters for various coordinate systems and is suited to emission and immunity testing both in the frequency and time domains.

10.6.1 Principles

The techniques used for NFS are constantly evolving and the universal exchange format must allow future techniques to be included without the need for complete remodeling. The format should also be portable between operating systems, as well as both human and machine readable. The XML format meets these

requirements perfectly. The use of keywords allows information to be included only as required. Additional keywords can be added to cater for new techniques, although they may not be interpreted by older software versions.
The ASCII representation of XML allows the files to be created modified and merged either manually, for example with text processors, or with simple scripts. Expensive specific software is not required for managing the files.
NFS techniques are used for measuring radiated emission and radiated immunity levels. The exchange format allows for both of these cases, but not in the same document, by enclosing all the information in a root XML element whose "Scantype" keyword may be either "EmissionScan" or ImmunityScan". A simple exchange file is shown in Fig. 10-1.

```
<?xml version="1.0" encoding="UTF-8"?>
<EmissionScan>
	<Nfs_ver>1.0</Nfs_ver>
	<Filename>Minimum_NFS_file.xml</Filename>
	<File_ver>1</File_ver>
	<Data>
		<Measurement>
			<List>
26e-3 29e-3 2e-3 -58
			</List>
		</Measurement>
	</Data>
</EmissionScan>
```

Figure 10-1 : Example file for scan emission

In order to ensure portability and compressibility, only relative paths can be used to define a path name. An absolute path is not exportable. All XML files concerning the NFS project must be placed in the same directory and other files containing data, pictures, documentation, etc must be placed in the same directory or in subdirectories.
The XML file is divided into sections concerning:

- Header information (filename, date, version, etc).
- Information about the component being scanned.
- Details of the measurement setup.
- Information on the probe (field, performance factor, etc).
- Data including the coordinate system used, frequencies or times and the data values.

Each section may be present, or not, and may include specific keywords allowing various parameters to be specified.

10.6.2 XML format in IC-EMC

The file « scan_component.xml» added to IC-EMC v2.5 (download at www.ic-emc.org) contains the following information :

```
<?xml version="1.0" encoding="UTF-8"?>
<EmissionScan>
    <Component>
    </Component>
    <Setup>
```

```
    </Setup>
    <Probe>
    </Probe>
    <Data>
    </Data>
</EmissionScan>
```

10.6.3 Remarks about the implementation of XML in IC-EMC

Keyword as defined in	Comments
<EmissionScan>	Opens the emission scan section
<Nfs_ver>	NFS template version; example 0.1
<Filename>	Document filename; example “scan_component.xml”
<File_ver>	Revision of the document file: example “1.0”
<Date>	The date of the file generation; example: 23 nov. 2007
<Source>	The XML data source; example “Freescale”
<Notes>	Notes added to the document
<Disclaimer>	Disclaimer information
<Copyright>	Copyright information
<Notes>	A notes section can be inserted anywhere in the file and the number of notes sections in the file is not limited.
<Component>	Opens the component section
<Component><Name>	Component name
<Component><Manufacturer>	Manufacturer description
<Component><Image>	Opens the Image subsection
<Component><Image><Path>	Link to the component image ; Example “component_image.JPG”
<Component><Image><Unit>	Image size unit; example “mm”
<Component><Image><Xsize>	Image size in X; example “81.0” (unit defined as mm)
<Component><Image><Ysize>	Image size in Y; example “82.0” (unit defined as mm)
<Component><Image><Xoffset>	Image shift in X
<Component><Image><Yoffset>	Image shift in Y
<Setup>	Opens the Setup section
<Setup><Config>	Opens the Configuration sub-section
<Setup><Config><Att>	Attenuation ; example: “0.0”
<Setup><Config><Average>	Average mode
<Setup><Config><Ref_level>	Reference level; example: “-10”; unit by default is dBm
<Setup><Config><Rbw>	Resolution Bandwidth; example: “3000.0” ; uniy by default is Hz
<Setup><Config><Vbw>	Video Bandwidth; example: “3000.0” ; uniy by default is Hz
<Setup><Config><Swp>	Sweep time; example: “0.143156653” ; unit by default is seconds
<Setup><Transducer>	Opens the Transducer sub-section. This section specifies information about cable losses and a preamplifier, if one is used during near-field scan.
<Setup><Transducer><Frequencies>	All information contained in this section concerns the frequencies at which the transducer gain data is listed.
<Setup><Transducer><Frequencies><Unit>	Specifies units of the frequencies at which the transducer gain data is listed.
<Setup><Transducer><Frequencies><List>	Specifies a list of frequencies at which the transducer gain is listed.
<Setup><Transducer><Gain>	Specifies a list of transducer gain values corresponding to the frequencies listed in the Frequencies sub-section of the Transducer section.
<Probe>	Opens the probe section
<Probe><Name>	Probe name; Example: “Freescale_Hz_1mm”
<Probe><Field >	Field measured with this probe; example: “HZ”
<Probe><Frequencies>	Opens the section that gives the list of frequencies available for

	each calibration point
<Probe><Frequencies><Unit>	Frequency unit of the probe calibration list
<Probe><Frequencies><List>	List of frequencies available for each calibration point; example "40E6 60E6 80E6 100E6 200E6 »
<Probe><Perf_factor>	Opens the probe performance factor section
<Probe><Perf_factor><Unit>	Unit of the probe performance factors
<Probe><Perf_factor><List>	List of probe performance factors according to frequency list; Example "-57.6 -54.5 -52.8 -50 -44 »
<Data>	Opens the data section
<Data><X0>	Absolute X coordinates of the scan
<Data><Y0>	Absolute Y coordinates of the scan
<Data><Z0>	Absolute Z coordinates of the scan
<Data><Xstep>	Added by B. Vrignon, E. Sicard to inform about the scan step in X axis
<Data><Ystep>	Added by B. Vrignon, E. Sicard to inform about the scan step in Y axis
<Data><Frequencies>	Opens the section that gives the list of frequencies available for each scan point
<Data><Frequencies><Unit>	Frequency unit
<Data><Frequencies><List>	Opens the frequency list; example (in Hz): 2290000.0 4580000.0 6870000.0 9160000.0 1.145E7 3.2E7 6.4E7 9.6E7 1.28E8 1.6E8
<Data><Times>	Specifies the Times section. All information contained in this section concerns the times at which the near-field scan data is measured.
<Data><Times><Unit>	Specifies units of the times at which the near-field scan data is listed.
<Data><Times><List>	Specifies a list of times at which the near-field scan measurement data is listed.
<Data><Measurement>	Opens the section that gives the measuring data
<Data><Measurement><Unit>	Measurement unit; example : "dBm"; default is dBm
<Data><Measurement><Unit_x>	Added to declare the X data unit.
<Data><Measurement><Unit_y>	Added to declare the Y data unit.
<Data><Measurement><Unit_z>	Added to declare the Z data unit.
<Data><Measurement><Data_files>	Specify the file path of data measurement
<Data><Measurement><List>	Opens the measurement list
26.0 29.0 2.0 -93.691 -93.726 -91.783 -90.772 -93.52 -91.865 -81.705 -78.408 -87.561 -92.142	X Y Z location in "unit_x".. unit (Example mm); followed by measured data (Unit in this example: "dBm") for each frequency defined in the Frequency list (here 10 values);

10.6.4 Notes

1. The numbers use "." Instead of ",". Example: -64.38
2. The separation between numbers is the SPACE character instead of « , »

10.6.5 Remarks about the hierarchy description

Recommendations have been proposed for a project architecture including several scan data (both emission and immunity), which gives some guidelines on how to store near-field scan files. Although beyond the scope of the XML standard which only focuses on basic keywords, these recommendations may eases the implementation of the standard. An example of how these files can be sorted in different folders has been proposed below:

```
+-- My Projects
|     +-- Project_name
|     |     |-- Project_name.xml
|     |
|     |     +-- EmissionScan
|     |     |     +-- Measurement 1
|     |     |     |     |-- Picture.jpg
|     |     |     |     |-- Dataxxx.xml
|     |     |     |     |-- Datayyy.xml
|     |     |     |     :
|     |     |     |
|     |     |     +-- Measurement n
|     |     |     |     :
|     |     :
|     |
|     +-- ImmunityScan
|     |     :
```

The file “Scan_Hx_PA_1950_1_5mm_PA_v2.xml”, contained in the directory “case study\pa_3g\Scan_Hx_PA_1950_1_5mm”, illustrates the implementation of XML using multiple data files. Figure 10-2 shows the picture resulting from the extraction of data included in this xml file in the Near Field Scan interface.


```
<?xml version="1.0" encoding="UTF-8"?>
<EmissionScan>
<Nfs_ver>0.50</Nfs_ver>
<Filename>Scan_Hx_PA_1950_1_5mm_PA_v2.xml</Filename>
<File_ver>1.00</File_ver>
<Date>18/05/2009 16:28:39 PM</Date>
<Source>Freescale</Source>
<Disclaimer>This file is used to save results of near field scan. Other use is not guaranteed.</Disclaimer>
<Copyright>This document is the property of FREESCALE Semiconductors SAS.</Copyright>
<Notes>Celine Dupoux, Samuel Akue Boulingui, Etienne Sicard</Notes>
<Documentation>See IEEE EMC Austin 2009 demo and paper</Documentation>
<Component>
  <Name>3G Power Amplifier</Name>
  <Manufacturer>Freescale</Manufacturer>
  <Criterion>High emission at 3G bandwidth</Criterion>
  <Image>
    <Path>pa_3g_3.bmp</Path>
    <Unit>mm</Unit>
    <notes>1 pixel= 0.06mm; image size 647x396</Notes>
    <Xsize>38.82</Xsize>
    <Ysize>23.76</Ysize>
    <Zsize>0.000000</Zsize>
    <Rsize></Rsize>
    <Hsize></Hsize>
    <Asize></Asize>
    <Bsize></Bsize>
    <Xoffset>-9.8</Xoffset>
    <Yoffset>-3.6</Yoffset>
    <Zoffset>0.000000</Zoffset>
    <Roffset></Roffset>
    <Hoffset></Hoffset>
    <Aoffset></Aoffset>
    <Boffset></Boffset>
  </Image>
</Component>
<Setup>
<Coordinates>-xyz</Coordinates>
<Config>
<Probe_signal></Probe_signal>
<Att>10.000000</Att>
<Average>OFF</Average>
<Ref_level>0.000000dBm</Ref_level>
<Rbw>1.000000kHz</Rbw>
<Vbw>1.000000kHz</Vbw>
<Swp>128.84100000000000800000000000ms</Swp>
<Xdiv></Xdiv>
<Ydiv></Ydiv>
<Bw></Bw>
<Coupling></Coupling>
</Config>
<Transducer>
<Frequencies>
<Unit></Unit>
<List></List>
</Frequencies>
<Gain></Gain>
</Transducer>
</Setup>
<Probe>
  <Name></Name>
  <Field>HX</Field>
  <Frequencies>
  <Unit></Unit>
  <List></List>
</Frequencies>
<Perf_factor>
<Unit></Unit>
<Unit_a></Unit_a>
<List></List>
</Perf_factor>
</Probe>
<Data>
<X0>10.20000mm</X0>
<Y0>5.0000mm</Y0>
<Z0>1.5000000mm</Z0>
<R0></R0>
<H0></H0>
<A0></A0>
<B0></B0>
<Xmax>23.000000mm</Xmax>
<Ymax>16.000000mm</Ymax>
<Zmax>1.500000mm</Zmax>
<Rmax></Rmax>
```

<Hmax></Hmax>
<Amax></Amax>
<Bmax></Bmax>
<Xstep>0.200000mm</Xstep>
<Ystep>0.200000mm</Ystep>
<Zstep></Zstep>
<Rstep></Rstep>
<Hstep></Hstep>
<Astep></Astep>
<Bstep></Bstep>
<Frequencies>
<Unit>MHz</Unit>
<List>1950
</List>
</Frequencies>
<Times>
<Unit></Unit>
<List></List>
</Times>
<Measurement>
  <Unit>dBm</Unit>
  <Unit_x>mm</Unit_x>
  <Unit_y>mm</Unit_y>
  <Unit_z>mm</Unit_z>
  <Unit_r></Unit_r>
  <Unit_h></Unit_h>
  <Format></Format>
<Data_files>
Scan_Hx_PA_1950_1_5mm_PA0.dat
Scan_Hx_PA_1950_1_5mm_PA1.dat
Scan_Hx_PA_1950_1_5mm_PA2.dat
Scan_Hx_PA_1950_1_5mm_PA3.dat
Scan_Hx_PA_1950_1_5mm_PA4.dat
Scan_Hx_PA_1950_1_5mm_PA5.dat
Scan_Hx_PA_1950_1_5mm_PA6.dat
Scan_Hx_PA_1950_1_5mm_PA7.dat
Scan_Hx_PA_1950_1_5mm_PA8.dat
Scan_Hx_PA_1950_1_5mm_PA9.dat
Scan_Hx_PA_1950_1_5mm_PA10.dat
Scan_Hx_PA_1950_1_5mm_PA11.dat
Scan_Hx_PA_1950_1_5mm_PA12.dat
Scan_Hx_PA_1950_1_5mm_PA13.dat
Scan_Hx_PA_1950_1_5mm_PA14.dat
Scan_Hx_PA_1950_1_5mm_PA15.dat
Scan_Hx_PA_1950_1_5mm_PA16.dat
</Data_files>
</Measurement>
</Data>
</EmissionScan>

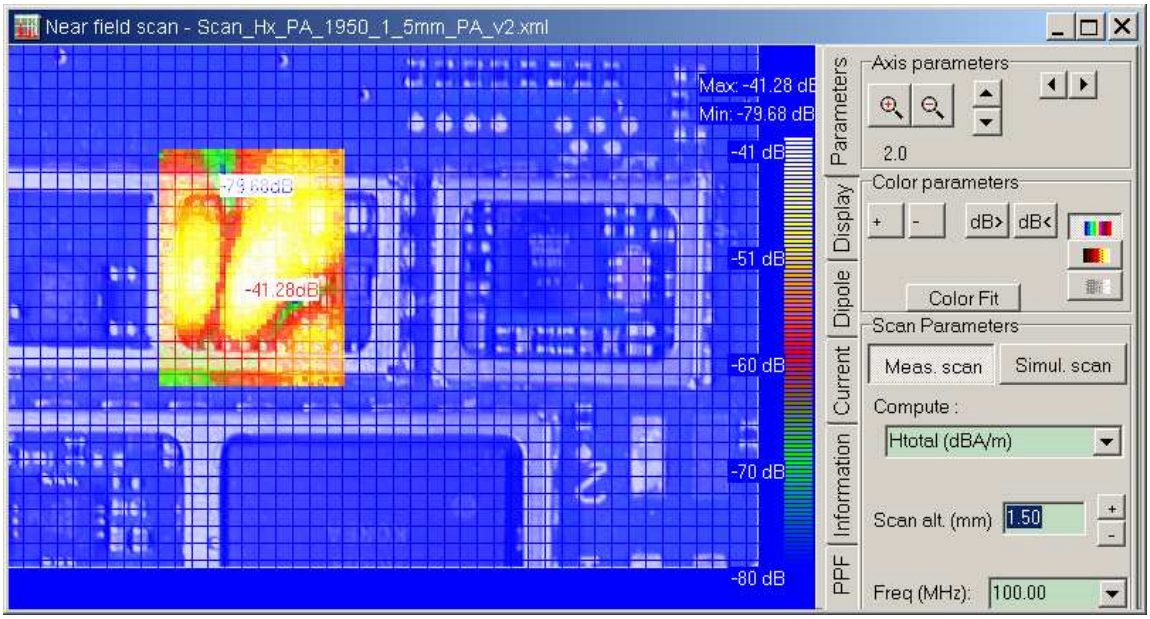


Figure 10-2 : The XML-based description of near-field scan data (case study\pa_3g\Scan_Hx_PA_1950_1_5mm)

When reading the XML file, the sub-item "Information" gives some indication about the data which has been decoded. We may see that IC-EMC loads several data files according to the main file request, through keyword <Data_files><Filename><Filename>..</Data_files>.

```
XML : ?xml version="1.0" encoding="UTF-8"?>
XML date 18/05/2009 16:28:39 PM
XML source Freescale
XML note :Celine Dupoux, Samuel Akue Boulingui, Etienne Sicard
XML - Image unit in mm
XML note :1 pixel= 0.06mm; image size 647x396
XML - Frequency unit in MHz
XML - Data unit in dBm
XML - X unit in dBm
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA0.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA1.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA2.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA3.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA4.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA5.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA6.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA7.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA8.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA9.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA10.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA11.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA12.dat"
XML - open subfile "Scan_Hx_PA_1950_1_5mm_PA13.dat"
```

10.7 References

[10-1] "Touchstone® File Format Specification – Revision 1.1", EIA/IBIS Open Forum, 2002

[10-2] J. Shepherd, A. Nakamura, F. Lafon, E. Sicard, M. Ramdani, D. Pommerenke, G. Muchaidze, S. Serpaud "Developing a Universal Exchange Format for Near-Field Scan Data", oral presentation at IEEE EMC Symposium Austin, Texas, USA, 2009, also on-line at www.ic-emc.org

11 Appendix B- Technology file example for configuring IC-EMC

.TEC file provides some basic information concerning a technology that can influence electromagnetic compatibility They are available in lib subdirectory. Table 11-1 lists the TEC files provided in IC-EMC and the targeted technology. The default TEC file is “default.tec”. The desired technology file should be renamed “default.tec” to configure IC-EMC at initialization.

Technology file	Description
Cmos12.tec	2 metal layers, 5V
Cmos08.tec	2 metal layers, 5V
Cmos06.tec	2 metal layers, 5V
Cmos035.tec	3 metal layers, 3.3V
Cmos025.tec	5 metal layers, 2.5V
Cmos018.tec	5 metal layers, 1.8V
Cmos012.tec	6 metal layers, 1.2V
Cmos90n.tec	6 metal layers, 1.0V
Cmos65n.tec	6 metal layers, 1.0V
Cmos45n.tec	8 metal layers, 1.0V

Table 11-1 : technology files used to configure IC-EMC

The following parameters are defined in the TEC file:

Parameter	Default value	Unit	Description
VDD	2.5	V	Configures the DC voltage for voltage sources
TCurrent	0.3e-3	A	Typical current per gate
Tdelay	0.1e-9	Second	Typical gate delay
Gactivity	0.1	0-1	Percentage of switching gate at each clock edge (0=0%, 1=100%)
Cdecap	7e-15	F	Elementary capa per gate
Csurf	15e-6	F/m2	IC default decoupling capa per mm2
Ldil	15e-9	H/lead	Serial parasitic inductance of DIL leads
Lqpf	10e-9	H/lead	Serial parasitic inductance of QFP leads
Lpga	15e-9	H/lead	Serial parasitic inductance of PGA leads
Lbga	5e-9	H/lead	Serial parasitic inductance of BGA leads
Lubga	4e-9	H/lead	Serial parasitic inductance of UBGA leads
Lcsp	2e-9	H/lead	Serial parasitic inductance of CSP leads
WN	2e-6	m	Default width size for nMOS devices
WP	10e-6	m	Default width size for pMOS devices

Table 11-2 : Technological parameters detailed in .tec file

One example of TEC file is given below:

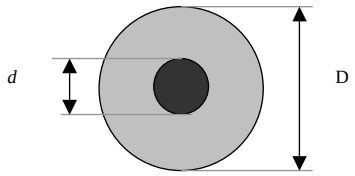
```
IC-EMC 2.5 - technology file
NAME "CMOS 0.25um"
VERSION 11.10.2004
* Supply voltage
VDD = 2.5
* Typical gate delay in ns
TDelay = 0.100
* Typical current in mA
TCurrent = 0.3
* Gate activity from 0 to 100 (%)
GActivity = 10
* Parasitic capa in fF per gate
Cdecap = 7
* Parasitic capa in pF/mm2
Csurf = 15
* Package inductance in nH/pin
LDIL = 15
LQFP = 10
LPGA = 7
LBGA = 5
LUBA = 4
LCSP = 2
* Default MOS length and width
ML  = "0.25u"
MW  = "2.0u"
*
* End cmos025.tec
*
```

12 Appendix C- EMC Model library

This appendix describes the models of some usual devices encountered in EMC measurement: cables, TEM cell, loop antennas, capacitors, inductors…. These models present some typical high frequency parasitic which affect these devices. Some of them are available in the EMC-lib subdirectory.

12.1 Cable model

The inductance and capacitance of a coaxial cable are given by equations 12-1 and 12-2, respectively [12-1].



$$L = \frac{\mu_0}{2\pi} ln \frac{D}{d} \qquad \textit{Equ. 12-1}$$

L = inductance (H/m)

$$C = \frac{2\pi\varepsilon_0 \varepsilon r}{ln\frac{D}{d}} \qquad \textit{Equ. 12-2}$$

C= capacitance (F/m)

The typical capacitance of a 50-Ω coaxial cable is around 100 pF/m. It decreases to 65 pF/m for 75-Ω cable, and 50 pF/m for twisted pairs. Coaxial cables may have 50Ω or 75Ω impedance. Twisted pairs may have Zc=100Ω (USA), or 120Ω (Europe).

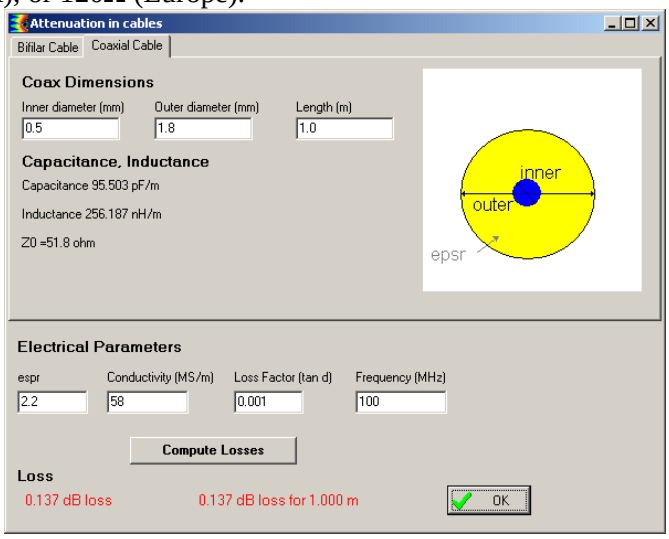


Figure 12-1 : Impedance and attenuation in cables (Tools→Attenuation in Cables)

The ohmic loss in the cable may be computed using Equ. 12-3 [12-2] and the dielectric losses may be computed using Equ. 12-4. To compute attenuation of these types of coaxial cable, click „**Tools → Attenuation in cables**“. The cable capacitance, inductance, impedance and loss appear as seen in Fig. 12-1.

$$ohmic\ loss\left(dB/m\right)=\frac{45.8e-6\times\sqrt{\varepsilon_r\times f}}{\ln\left(\frac{d_{out}}{d_{in}}\right)}\times\left(\frac{1}{d_{in}\times\sqrt{\sigma}}+\frac{1}{d_{out}\times\sqrt{\sigma}}\right)\quad Equ.\ 12\text{-}3$$

$$dielectric\ loss\left(dB/m\right)=91e-9\times\sqrt{\varepsilon_r}\times f\times\tan\delta\quad Equ.\ 12\text{-}4$$

where
d_{in}: diameter of inner conductor
d_{out}: diameter of dielectric tube
ε_r: dielectric constant
σ: conductivity of metallic conductors
tan δ: loss factor

It can be noticed that attenuation increases with frequency. In low frequency, ohmic losses dominate while dielectric losses dominate in high frequency. RG402 and RG405 are two semi-rigid coaxial cable typically used in EMC measurement. Table 12-1 gives geometrical and electrical parameters of these cables.

Cable type	RG 402	RG 405
Inner diameter (mm)	0.92	0.515
Dielectric diameter (mm)	2.98	1.68
εr, dielectric material	2.1	2.1
Σ (MS/m)	58	58
tan δ	0.00045	0.00045
Loss at 5 GHz (dB/m)	0.92	1.51

Table 12-1 : Geometrical and electrical parameters of different types of coaxial cables

12.2 TEM model (valid up to 1GHz)

Figure 12-2 presents a simple electrical model of TEM cell. The validity of this model in the frequency domain is linked to the quasistatic approximation limitation, which is valid until the length of the line (here the septum of the TEM cell) is inferior or equal to the tenth of the wavelength. It can be noticed that the ratio between TEM inductance and capacitor is equal to 50 Ω.

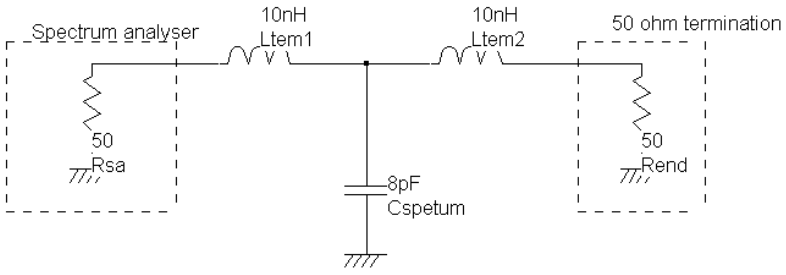


Figure 12-2 : TEM Cell model (EMC_lib\temModel.sch)

12.3 RLC Line

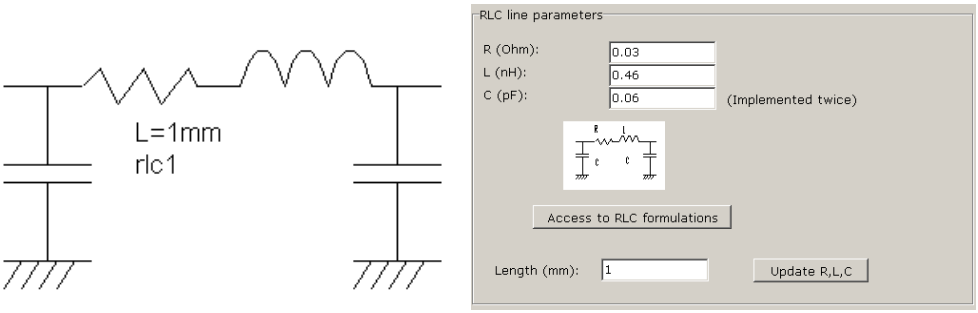


Figure 12-3 : RLC model

The RLC symbol  is composed of one serial resistance, one serial inductance and two capacitors to the ground, in a pi-model form. The values may be user defined or computed from the R,L,C formulations accessible from the menu "**Tools → Interconnect Parameters**".

12.4 Oscilloscope Model

In immunity tests, an oscilloscope can be used to monitor a given signal which serves as a susceptibility criterion. The attachment between the device under test and the oscilloscope and the oscilloscope input can directly influence the measured susceptibility. Three cases are considered:

- 50 Ω load oscilloscope input: in this mode, the oscilloscope input matches the cable characteristic impedance. It is recommended for radio-frequency measurements but it influences strongly the DUT. Indeed, this load absorbs current so it can influence the output of a digital circuit (e.g. a 50 ohms load connected to an ideal digital output supplied under 5 V absorbs 100 mA). Moreover, the oscilloscope input impedance can form with DUT impedance a voltage divider which influences the measurement
- High Impedance input: this is most common setup as it does not absorb DC current. As oscilloscopes are usually connected to the DUT using 50 Ω cables, the load presented to the DUT varies at high frequency. At the resonance of the cable, the load seen at the input of the cable tends to zero. For example, for a 50 ohms 1m coaxial cable, a resonance occur at 50 MHz. Cable resonances can affect the noise amount in the DUT due to total reflections at oscilloscope input.
- Active probe: these probes capture the signal close to the DUT and present a small load (e.g. 1.6pF load). Active probes are the preferred methods to monitor signals at circuit level as it prevents from disturbing the DUT due to a small load and cable resonances.

Models of these different probes are shown on figure 12-4. The oscilloscope is connected to the DUT with a 1-meter long 50 Ω cable. Three probes are used to measure the voltage across a load for varying frequencies. The original signal is 1 V generator connected to a 150 Ω serial resistance.

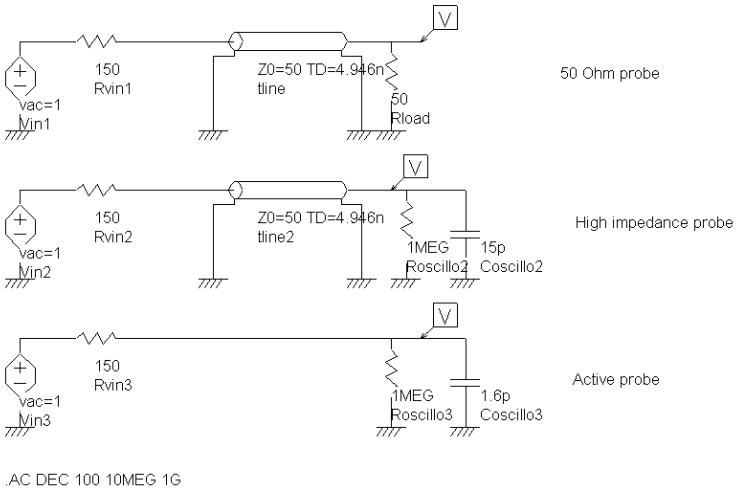


Figure 12-4 : Comparison between different probes (EMC_lib\probes_comparison.sch)

The ideal probe should give 1V over the whole frequency range. Figure 12-5 presents the simulation of the transfer functions of the different probes. The 50 Ω input greatly influences the measured value as it forms a voltage divider with the source resistance. However, the value is independent of the frequency because of the matching. When the oscilloscope is in high impedance, resonances and anti resonances at frequencies linked to multiples of λ/4 may be observed. The voltage measured by the oscilloscope becomes frequency dependent. Active probe has a quasi-ideal behaviour up to 100 MHz. The 3 dB cut-off frequency appears at 700 MHz.

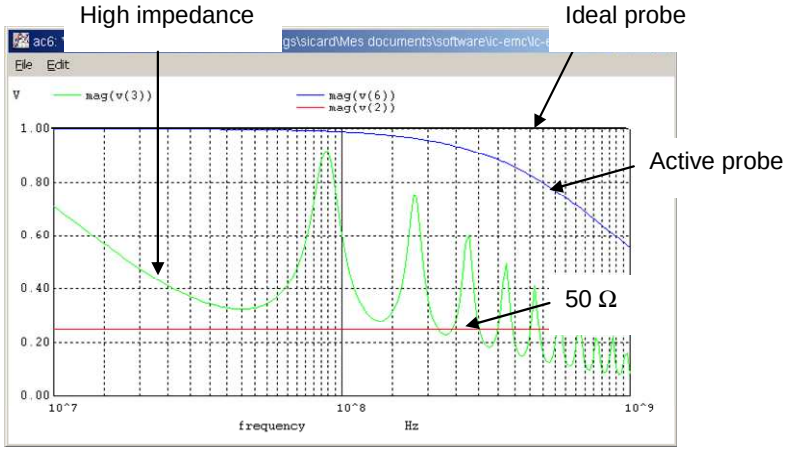


Figure 12-5 : Comparison of the transfer function of different probes (misc\probes_comparison.sch)

12.5 Capacitor Model

A surface-mounted capacitor has been characterized by L. Giacotto [12-3] in terms of impedance up to 10GHz. The corresponding model is given in Fig. 12-6. The comparison between measured (passive\capa_100pF_S22.s50) and simulated impedance is given in fig 12-7. A first resonance occurs at 450 MHz due to the parasitic inductance of the capacitor. A second resonance appears at 6.5 GHz due to the parasitic inductor and a parasitic parallel capacitor. The simple RLC model is valid up to 3 GHz. Parallel capacitor is required at higher frequency.

As explained in chapter 3 – Basic Concepts, parasitic electrical elements of electronic devices must not be neglected to model correctly the high frequency behavior. This example shows that this capacitor can not decouple correctly above 500 MHz because it is not a capacitor anymore. Moreover, as this decoupling capacitor is connected to the power supply of a circuit by PCB tracks, vias and package lead, a large parasitic inductance should be added which limits the decoupling efficiency of this capacitor above several tens of MHz.

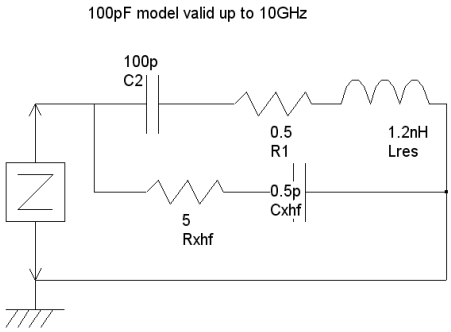


Figure 12-6 : 100-pF capacitor model extracted from [s] measurements (passive\capa_100pf_xhf.sch)

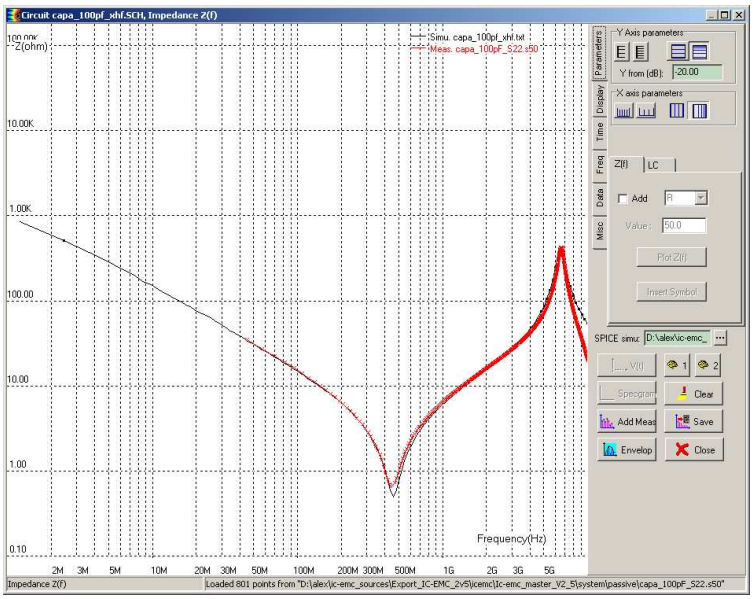


Figure 12-7 : comparison between measured and simulated impedance of a discrete 100-pF SMD capacitor (EMC_lib\passive\capa_100pf_xhf.sch)

12.6 Inductor and ferrite inductor models

Inductors and ferrite inductors (also known as ferrite beads or ferrites) are passive components commonly used on printed circuit boards to block and filter high frequency noise. As capacitors, ferrites and inductors present a frequency dependent model and have a limited frequency range, so that it is very important to know their models. Even if the use of these both components is similar, they are very different. While inductors are mainly formed of wire coils, ferrites inductors are made of a coil around a ferrite core. Inductors present an inductive behavior at low frequency, i.e. until the parasitic capacitors between wires of the coil resonates with the inductance of the coil. Therefore, the frequency range of an inductance is limited by the parasitic capacitor.

The principle of a ferrite is more complicated. At low frequency, the ferrite behaves like an inductor because of the coil. However, at higher frequency, the effect of a ferrite core becomes predominant. The ferrite core dissipate magnetic field due to high frequency noise to heat. Thus, at high frequency, the ferrite is equivalent to a resistor and can present to the noise a higher impedance than inductor. This property allows ferrite inductors to filter efficiently over frequency range on which inductors can not filter anymore. Of course, stray capacitors exist in ferrite inductor so that the frequency range of ferrites presents also a limitation.

S11 parameters measurements have been performed on an inductor and a ferrite in order to compare their behavior. The inductor model is a Wuerth Electronik WE-PD4 47 µH surface mounted inductor, the datasheet gives a resonant frequency equal to 12 MHz. The ferrite model is Murata BLM18HK102SN1 surface mounted ferrite inductor in a 0603 case, dedicated to filtering noise over the band 1 MHz – 1 GHz. From S11 measurements, models of both components were extracted by F.

Lafon. Figure 12-8 describes the model of the 47 µH inductor. The inductor presents a serial resistor that limits the quality factor, and a parallel parasitic capacitor due to stray capacitor. Figure 12-9 presents the comparison between the S11 measurement and simulation of the 47 µH inductor in a Smith chart (on the left), and between the Z11 measurement and simulation (on the right). Measurement is included in the file L47u_Z11meas.s1p. A strong resonance appears at 13 MHz, which confirms datasheet information.

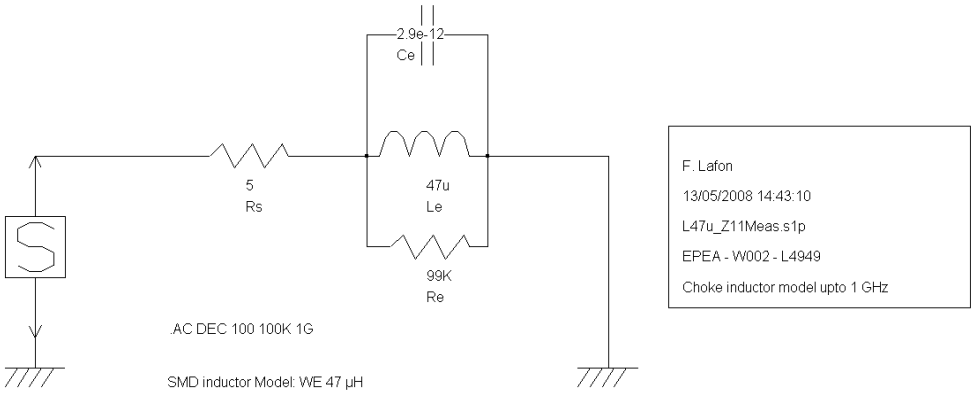


Figure 12-8 : Model of a 47 µH surface mounted inductor (passive\S11_L47u.sch)

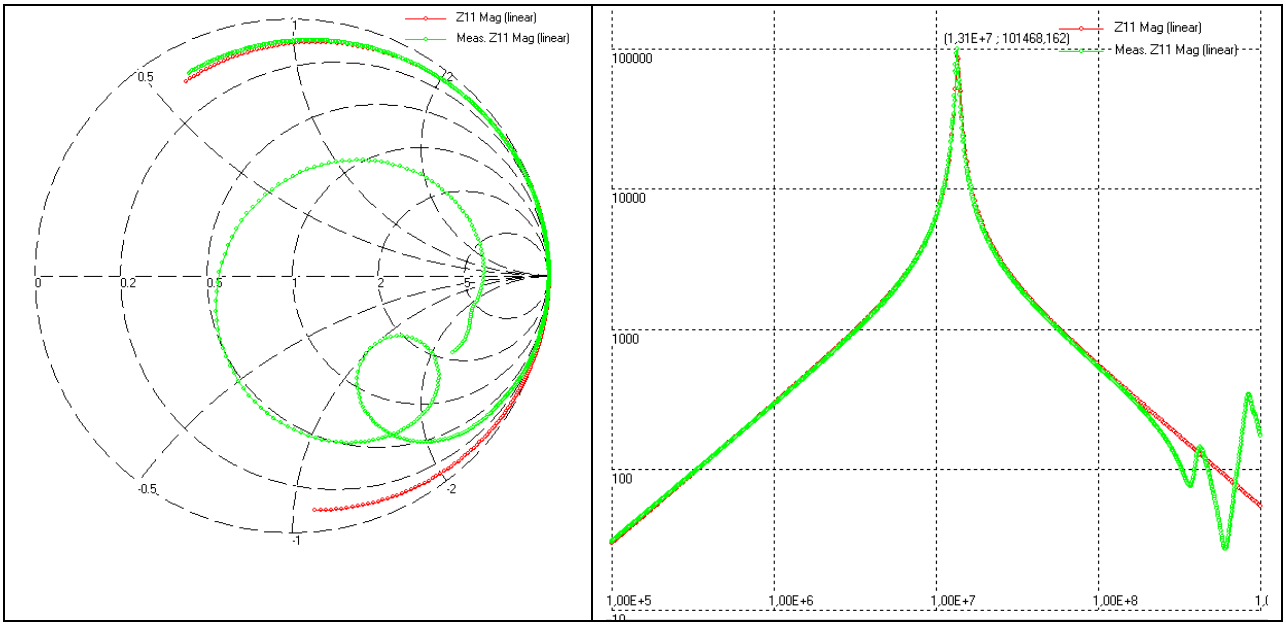


Figure 12-9 : Comparison between measurement and simulation of a 47 µH inductor (passive\ L47u_Z11meas.s1p)

Figure 12-10 describes the model of the ferrite. The model is more complex with several parallel R and L cells in order to exhibit an inductive effect at low frequency and a resistive behavior at higher frequency. The total inductor in low frequency is equal to 15 µH. A 0.2 pF stray capacitor bypasses resistors and inductors of the ferrite to model the behavior at very high frequencies. Figure 12-11 presents the comparison between the S11 measurement and simulation of the ferrite in a Smith chart (on the left), and between the Z11 measurement and simulation (on the right). Measurement is included in the file ferrite_Z11meas.s1p. The model reproduces correctly the behavior of the ferrite over all the frequency range.

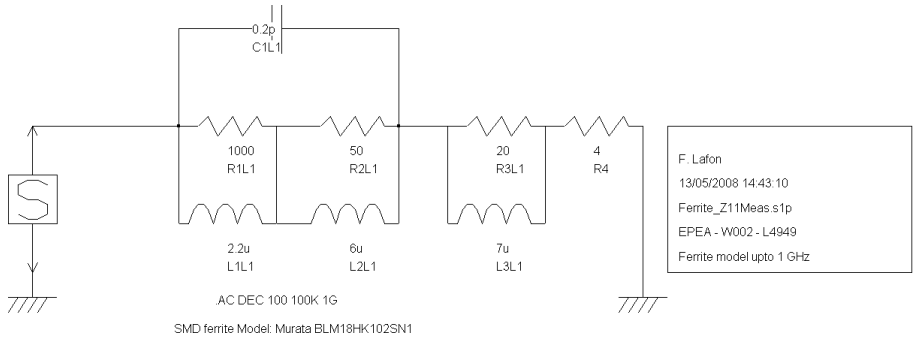


Figure 12-10 : Model of a surface mounted ferrite (passive\S11_Ferrite.sch)

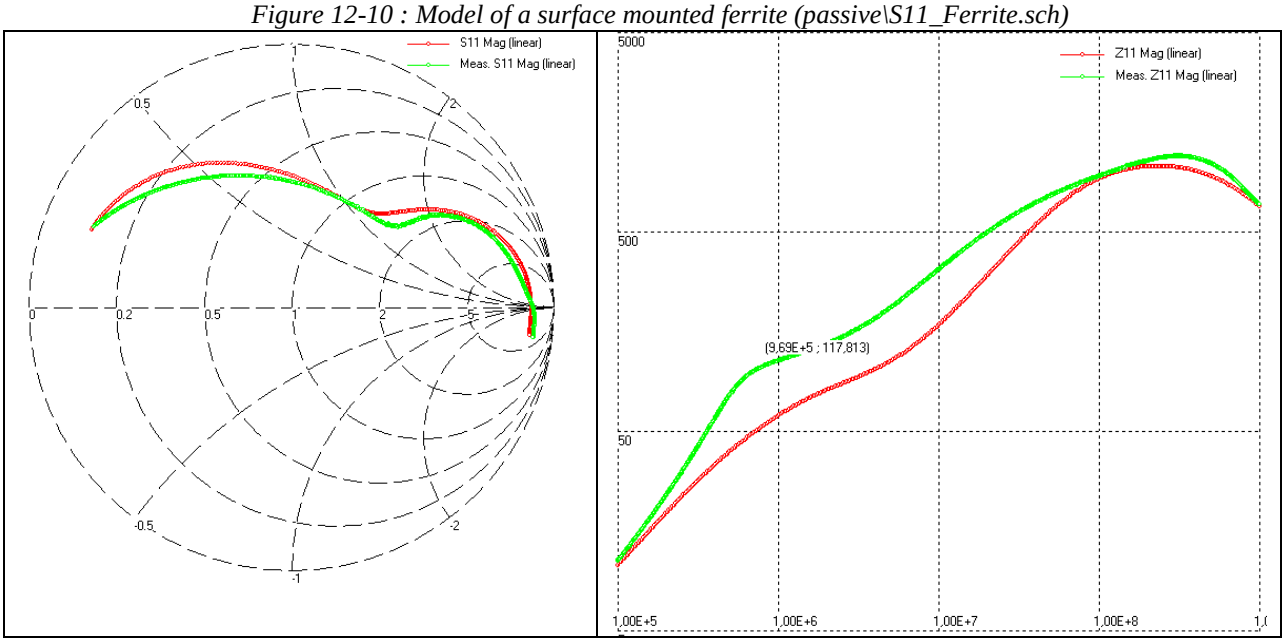


Figure 12-11 : Comparison between measurement and simulation of a ferrite inductor (passive\ ferrite_Z11meas.s1p)

These simulations and measurements confirm clearly the difference between an inductor and a ferrite. The inductor can present a very high impedance, but only on narrow band around the resonant frequency, while the ferrite presents a more constant and high impedance over a large frequency range.

12.7 Bias tee model

A bias tee is a decoupling network used to superimpose a low frequency signal and a high frequency signals. The bias tee ensures the isolation between the low frequency and the high frequency generators. A bias tee is required in Direct Power Injection (see 7.6 Direct Power Injection) in order to superimpose a conducted aggression on a low frequency signal (input signal or power supply). It takes the form of a 3 port devices composed of a low frequency (LF) input, a radiofrequency (RF) input and the output with the signal resulting of the superposition of both inputs. The LF input is isolated from RF signal by a device which cut high frequency signal, as resistor, inductor or ferrite. Resistors should be avoided if DPI is conducted on a power supply because of the power dissipation and the voltage divider effect. The RF input is isolated from low frequency signal by a device which cut low frequency signal, as a capacitor. Figure 12-12 presents a “home made” bias tee dedicated to DPI test on the frequency range 10 MHz – 3 GHz. This bias tee is mounted on a PTFE substrate board. Input and output SMA connectors are connected by 50 Ω microstrip line. A 1 nF capacitor and a 1 µH inductor isolate RF and LF input from each other.

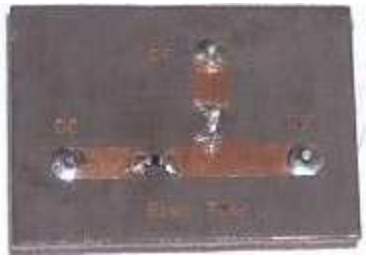


Figure 12-12 : Bias tee mounted on a specific board

Values of inductors and capacitors are optimized in order to give the following properties to the bias tee:

- A small reflection coefficient at RF input over all the targeted frequency range. It should be inferior to -10 dB to reduce input return loss.
- A high transmission coefficient from RF input to output over all the targeted frequency range. It should be greater than -3 dB to enhance RF transmission to the output.
- A high isolation or transmission coefficient from RF input and LF input over all the targeted frequency range. It should be less than -10 dB to prevent from RF leakage to LF source.

S parameter measurements were conducted on the bias tee presented in figure 12-12 and an electrical model were extracted. Figure 12-13 describes the model. Models of microstrip line are lossless 50 Ω transmission line, their delay time have been computed from physical length and dielectric constant of the substrate. The capacitor and inductor models are similar to those presented in figures 12-6 and 12-8. A parasitic serial inductor is added to the capacitor while a parallel capacitor is added to the inductor in order to limit their frequency behavior. Resistances are added to reduce their quality factors. Three enabled S ports are placed at each terminal of the model so that the complete 3×3 scattering matrix can be simulated. Figures 12-14 presents the comparison between measurement and simulation of the transmission coefficient between RF and OUT and the RF input reflection coefficient. Simulations fit satisfactorily with measurements. Results confirm that the bias tee has the required properties over the band 10 MHz – 3 GHz.

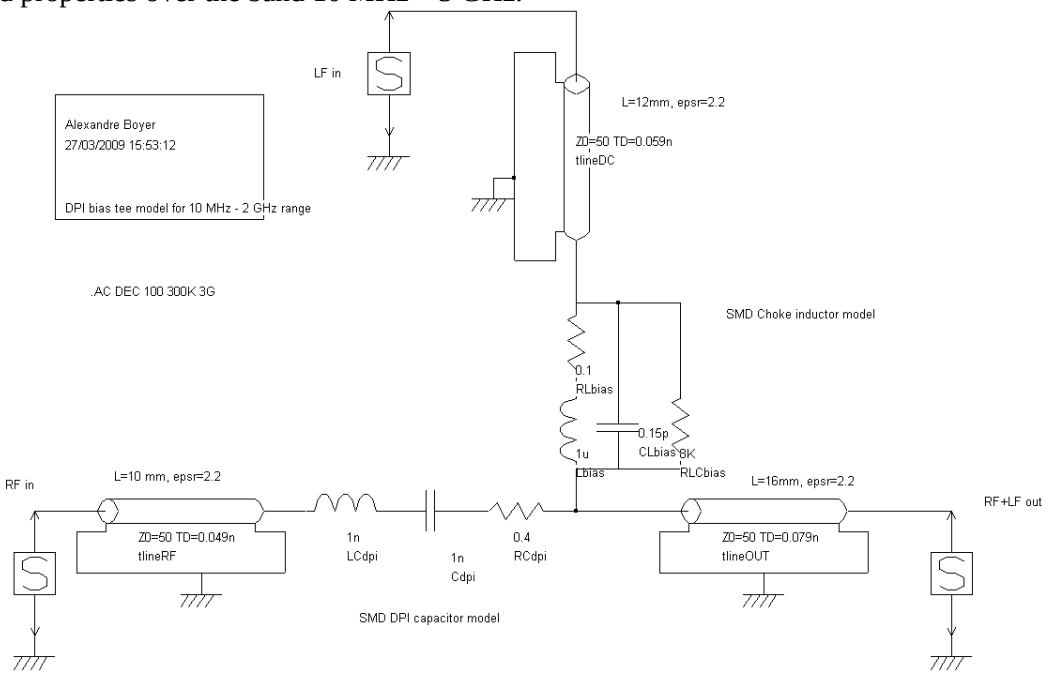


Figure 12-13 : Model of a bias tee optimized for the frequency range 10 MHz – 3 GHz (EMC_lib\3_port_bias_tee.sch)

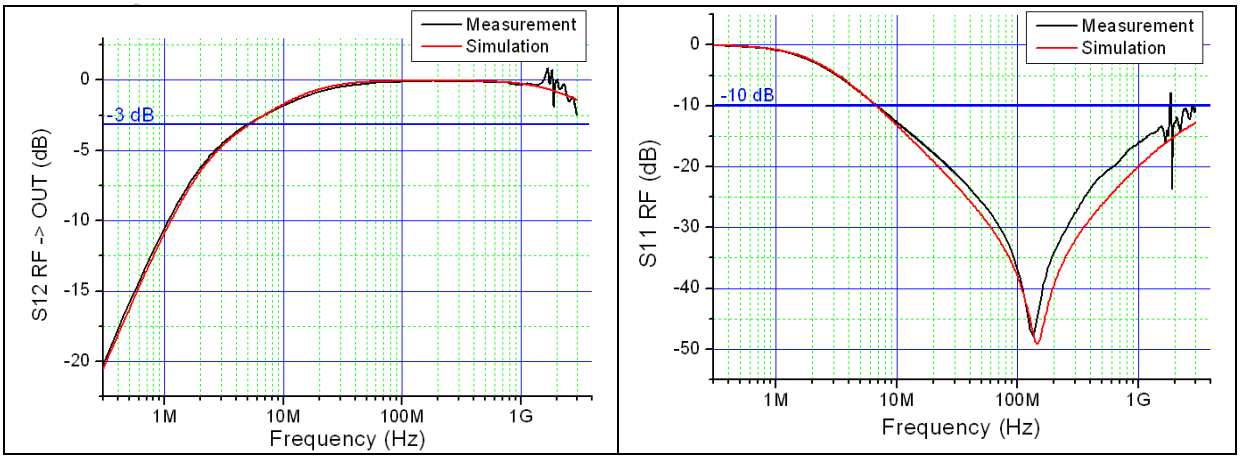


Figure 12-14 : Comparison between measurement and simulation of transmission between RF (on the left) and output and RF input reflection (on the right) (EMC_lib\3_port_bias_tee.sch)

12.8 Loop model

Loop antennas are basic antennas usually used as near field antenna. Even if its antenna factor is not constant over frequency, it can be considered as a magnetic wideband antenna, because it is a magnetic antenna up to its self resonance. The loop can be electrically modeled as a L C circuit. The L,C and corresponding resonant frequency of a small magnetic loop may be evaluated using the screen accessible through the command "Tools → Interconnect Parameters" as shown in Fig. 12-15. Equations 12-5 and 12-6 give equations to compute the self inductor and capacitor of a loop knowing its geometrical dimensions [12-4].

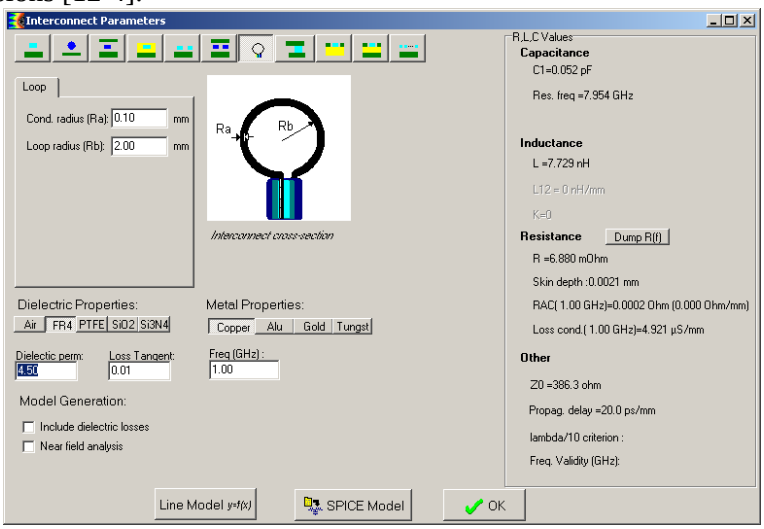


Figure 12-15 : Loop LC model

$$L = \mu_0 \mu_r b \left(\ln\left(\frac{b}{a}\right) - 2 \right) \qquad \textit{Equ. 12-5}$$

$$C = \frac{2\varepsilon_0 \varepsilon_r}{\ln\left(\frac{b}{a}\right) - 2} \qquad \textit{Equ. 12-6}$$

b: loop radius
a: wire radius

12.9 Skin Effect Model

The skin effect is a well-known physical phenomenon which increases the DC resistance of

interconnects at high frequencies. The skin effect corresponds to charges which are pushed on the periphery of the conductor, in such a way that the current density within the conductor is no more constant. The current density at the center of the connector tends to zero, thus increasing the global resistance of the conductor (figure 12-16).

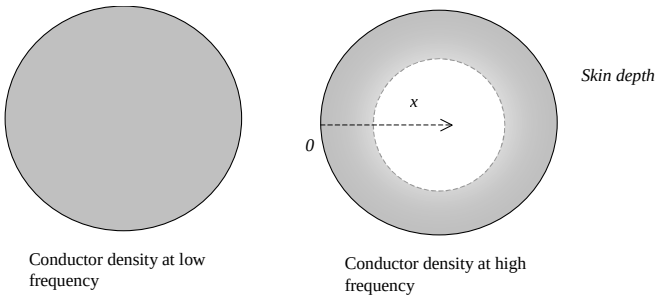


Figure 12-16: illustration of skin effect

The current density can be expressed by a the formulation below

$$J(z) = J_0 \, e^{-\frac{x}{\delta}} \qquad \textit{Equ. 12-7}$$

where
J_0 is the equivalent current density
x = depth in the conductor (m)
δ = skin depth (m)

The skin depth is expressed by

$$\delta = \sqrt{\frac{1}{\pi f \mu_0 \gamma}} \qquad \textit{Equ. 12-8}$$

where
f is the signal frequency (Hz); μ_0 = 1.257e^{-10} H/m, permittivity of vaccum
γ = conductivity (58.0 10^6 S/m for copper, 45.5 10^6 S/m for gold)

For gold, the skin depth at 1GHz is 2.4 µm. For a bonding (25µm diameter), this means that a 1 GHz signal is flowing only in a reduced section of the conductor, thus increasing significantly its equivalent resistance (Figure 12-17).

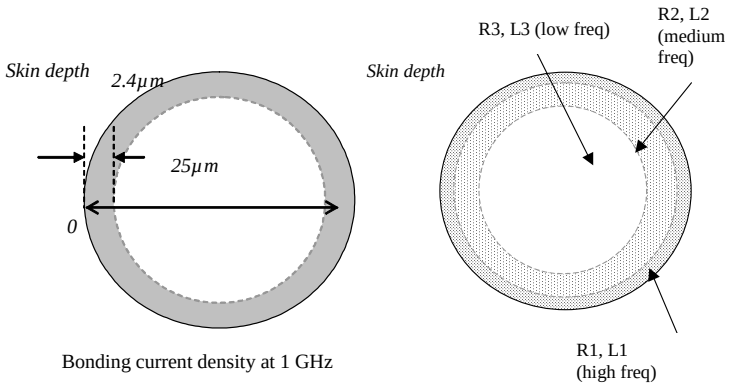


Figure 12-17 : Bonding wire at 1GHz and proposed model

From a simulation point of view, the skin effect may be handled using a set of R-L components, as illustrated in figure 12-18. At low frequency, the current flows through all the conductor section. At

medium frequencies, the high impedance value of L3 makes the current flow preferably through R2, L2 and R1,L1, which corresponds to a very low current density at the center of the conductor. At 1GHz, most of the current flows at the outer art of the conductor, this is modeled by R1, L1. Wheeler [12-5] recommends the use of the following ration for Rn and Ln :

$$R_n = R_0 \sqrt{10^n} \qquad \textit{Equ. 12-9}$$

$$L_n = L_0 \frac{1}{\sqrt{10^n}} \qquad \textit{Equ. 12-10}$$

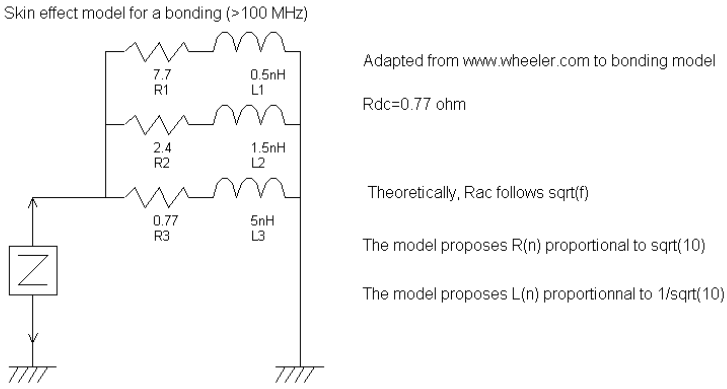


Figure 12-18 Skin effect model for a bonding wire (EMC_lib\skin_effect_bonding.sch)

The bonding model is proposed in figure 12-18. Three R, L paths have been placed in parallel. From the impedance simulation (10 MHz-10 GHz) reported Fig. 12-19, we observe a 10 dB increase of the conductor impedance, with a DC value close to 0.7 Ω. Around 1 GHz, the DC value is almost 7 Ω, 10 times the DC value.

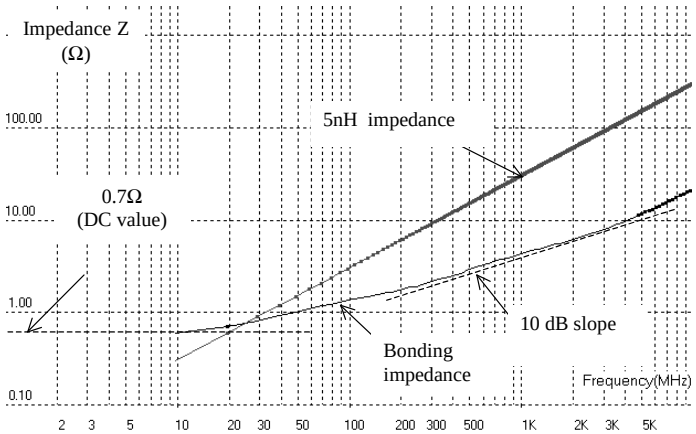


Figure 12-19 : Z(f) simulation showing the 10 dB frequency increase above 200 MHz (skin_effect_bonding.sch)

12.10 References

[12-1] B. C. Wadell, « Transmission Line Handbook », Artech House, ISBN 0-89006-436-9, 1991

[12-2] P. F. Combes, “Micro-Ondes – Lignes, Guides et Cavités”, Dunod, ISBN 2-10-002840-5, 1996

[12-3] L. Giacotto, PhD Thesis, 2002, INPG Grenoble, France

[12-4] M. Kanda, “Standard Probes for Electromagnetic Field Measurements”, IEEE Transactions on Antennas and Propagation, vol. 41, no 10, October 1993

[12-5] C. S. Yen, Z. Fazarinc, R. L. Wheeler, « Time-Domain Skin Effect Model for Transient Analysis of Lossy Transmission Lines », Proceedings of the IEEE, Vol. 70, No. 7, July 1982.

13 Appendix D – S parameter deembedding

S parameter measurements are usually used to extract equivalent passive models for passive or active circuits. S11 measurement allows the extraction of the input impedance of a device. However, devices under test are often mounted on special test board dedicated to characterization, with its input/output port connected to the VNA port by short 50 Ω lines and coaxial connectors. In that kind of condition, the calibration plane is not set at the DUT I/O level but at the input of the test board coaxial connectors. Therefore the S parameter measurements will suffer from the spurious effect of feed lines, especially at high frequency. If the attachment lines are electrically longer than the DUT, extraction of a model from S11 measurement will be difficult because of the inaccuracy introduced by the lines.
The first solution to extract correctly is to perform measurement directly on the DUT with coaxial probe. This solution is possible only for small device with few power supply and input pins. For a large circuit as a microcontroller with several power supply pairs, this type of measurements becomes costly. The second solution keeps the board mounting options and is based on a deembedding of the "raw" measurements. The deembedding consists in removing the effects of transmission lines and coaxial connectors mathematically. If the response of feed lines between calibration plane of the VNA and input of the DUT is known, mathematical operations can transform the original measurement to place virtually the calibration plane directly at the input of the DUT.
This appendix provides some theoretical elements of the deembedding process and describes briefly the S parameter deembedding tool proposed by IC-EMC.

13.1 Theory

An attachment lines modify the input impedance or a reflection coefficient seen from the input of a 1-port device because it can attenuate the signal or add phase. Here, we only consider 2 port attachment lines.

13.1.1 Perfectly matched attachment line

First, we consider the case where a perfectly matched line is added between the calibration plane of the VNA and the input of the DUT, as described in figure 13-1. This line only adds an extra phase to the measured reflection coefficient S_{11meas}. This phase must be removed to deduce the reflection coefficient S11 at the DUT input.

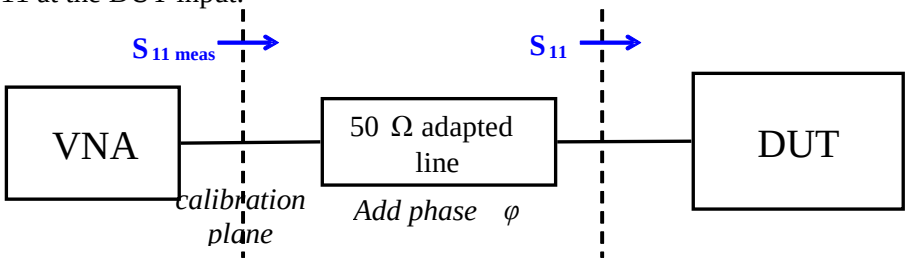


Figure 13-1 : The DUT input is connected to the VNA by a perfectly matched line (here the characteristic impedance Zc = 50 Ω)

Equation 13-1 gives the relation between S11 and S_{11mes}. R and X are the real and imaginary parts of S_{11mes}. Equation 13-2 gives the relation between the phase added by the line and its characteristics.

$$S_{11} = \frac{S_{11\,mes}}{\exp(-j2\varphi)} = (R\times\cos(2\varphi) - X\times\sin(2\varphi)) + j\times(R\times\sin(2\varphi) + X\times\cos(2\varphi)) \quad \textit{Equ. 13-1}$$

$$\varphi = \frac{2\pi L}{\lambda} = \frac{2\pi L f \sqrt{\varepsilon_r}}{c} = 2\pi f T_D \qquad \textit{Equ. 13-2}$$

where

L: the length of the feed line
Td: time duration induced by the line
εr: the dielectric constant
f: frequency

From the delay introduced by the line or its physical length, the phase added by the line can be computed at each frequency and S11 at the DUT input can be extracted fro S_{11mes}.
However this case is ideal. Even if a line is matched, the matching is never perfect (component insertion loss, dielectric losses, parasitic coupling… add some mismatch) so that this method is limited.

13.1.2 Unmatched attachment line

The second case concerns any kind of 2-port attachment line, as descried in figure 13-2. Reflection and transmission coefficients of the line were fully characterized with a VNA. Here Γ_L is the reflection coefficient at the DUT input.

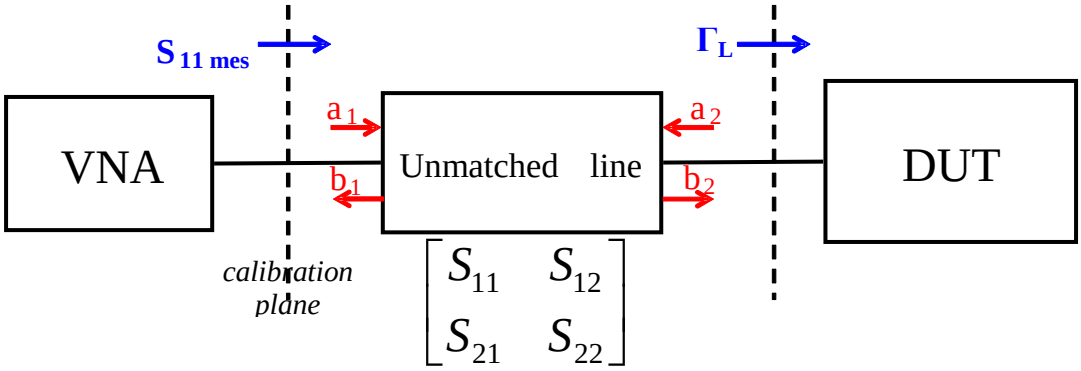


Figure 13-2 : The DUT input is connected to the VNA by a unmatched line fully characterized

Equations 13-3 and 13-4 detail the relation between S_{11mes} and Γ_L.

$$S_{11\,mes} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12} \times S_{21} \times \Gamma_L}{1 - S_{22} \times \Gamma_L} \qquad \textit{Equ. 13-3}$$

$$\Gamma_L = \frac{S_{11\,mes} - S_{11}}{S_{12} \times S_{21} + S_{22} \times \left(S_{11\,mes} - S_{11}\right)} \qquad \textit{Equ. 13-4}$$

Knowing the characteristics of the attachment line from a full two port measurement, the reflection coefficient of the DUT input can be extracted from the raw S11 measurement.

13.2 IC-EMC deembedding process

IC-EMC proposes a deembedding tool (command “Tools → S Parameters Deembedding”) which considers the two previous cases. The following chart explains the general flow for the deembedding process.

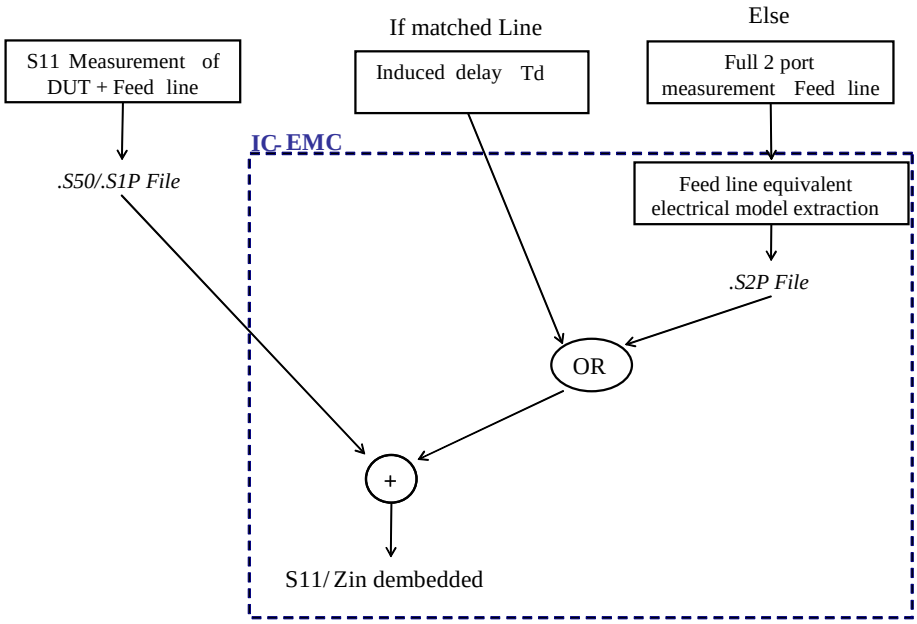


Figure 13-3 : Flow chart describing the deembedding process proposed by IC-EMC

13.3 Case study

Let's consider the simple RLC circuit described in figure 13-4 to illustrate the principle of the deembedding process. This circuit is the load that we want to characterize. Figure 13-5 presents the simulation of Z11. The LC resonance appears at 500 MHz.

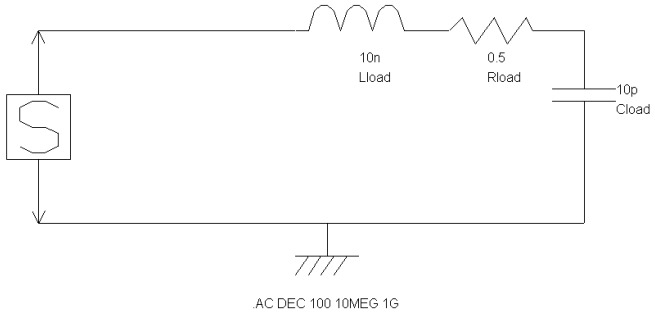


Figure 13-4 : S11 simulation of a RLC load (Basic\deembed\S11_LoadDeembed.sch)

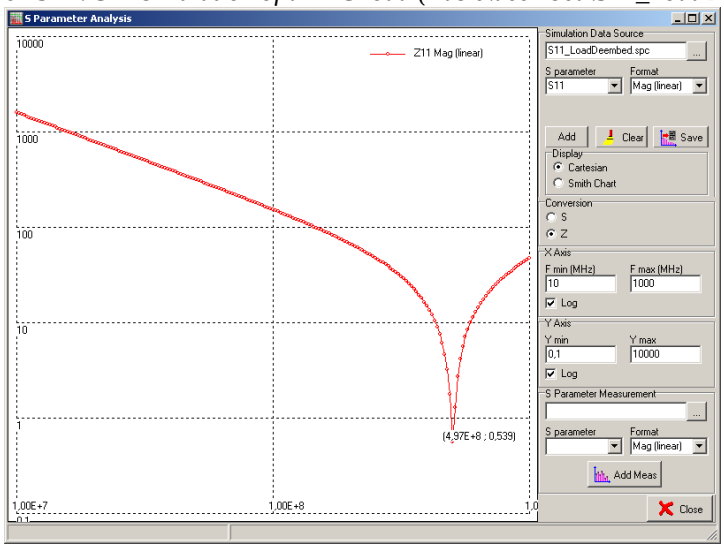


Figure 13-5 : S11 simulation of a RLC load (Basic\ deembed\S11_LoadDeembed.sch)

An unmatched line is used to connect the previous RLC load to a VNA. This line must be characterized to deembded the reflection coefficient of the load from the raw S11 measurement.

Figure 13-6 describes the schematics used to perform a full two port characterization of this line.

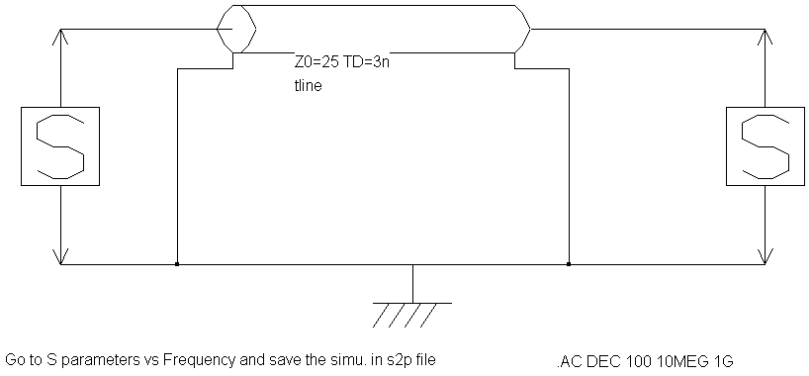
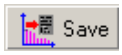


Figure 13-6 : Full two port characterization of an unmatched line (Basic\ deembed\Full2Port_LineDeembed.sch)

Launch WinSPICE simulation and then open the S parameter interface ("EMC → S Parameters"). Ensure that "Full2Port_lineDeembed.spc" is written in the field "Simulation Data Source" and that "Conversion" box is set at S. Click on the button 

to export simulation results in a .s2p file. The simulation results of the full two port characterization of the line can be found in the file "Full2Port_lineDeembed.s2p".
This line is now used to connect the RLC load to a VNA and measure the reflection coefficient. Figure 13-7 presents the schematic of this measurement. Open the file "basic\ deembed\S11_rawDeembed.sch". Be sure that the AC frequency sweeps are similar in the full two port characterization of the attachment line and in the raw S11 simulation. Launch WinSPICE simulation and then open the S parameter interface. AS previously, export the S11 simulation in a .s1p file ("basic\ deembed\S11_rawDeembed.s1p") and close the S parameter interface.

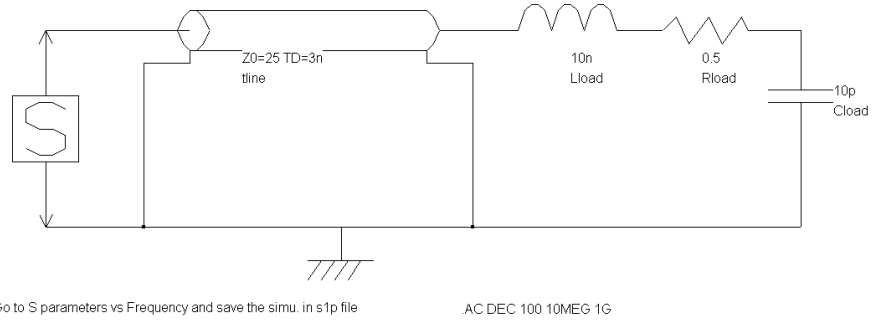


Figure 13-7 : S11 characterization of a RLC load connected to a VNA port by an unmatched line (Basic\ deembed\S11_rawDeembed.sch)

Open the deembedding tool (command "Tools → S Parameters Deembedding"). Figure 13-8 presents the interface of this tool. In the field "Measurement to deembed", seelct the file related to the S11 raw measurement called "basic\ deembed\S11_rawDeembed.s1p" and click on the button "Load". The raw measurement is plotted on the right part of the screen, in a Z11 form.

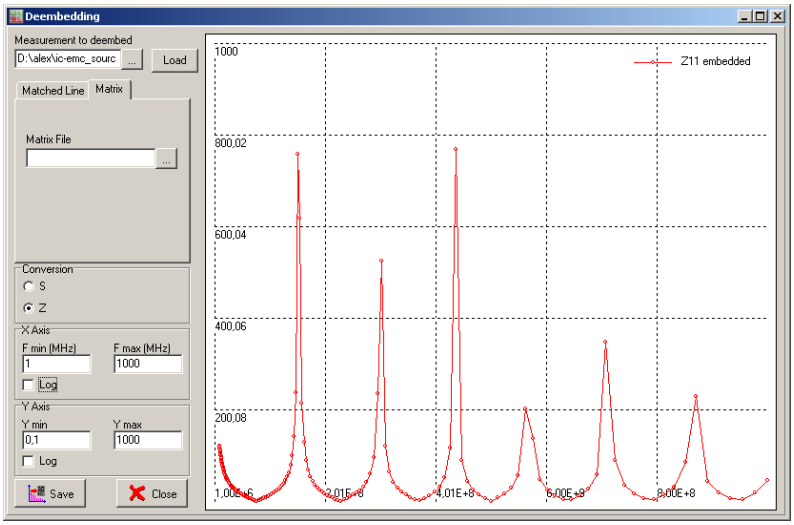


Figure 13-8 : S11 characterization of a RLC load connected to a VNA port by an unmatched line (Basic\ deembed\S11_rawDeembed.sch)

Two tabs appear on the left part of the screen: “Matched Line” and “Matrix”. They correspond to the two deembedding configurations. Choose “Matrix” options and import the file “basic\ deembed\Full2Port_lineDeembed.s2p”. Automatically, the deembedded reflection coefficient is plotted on the graph, in a Z11 form as illustrated in figure 13-9. Use the different buttons to configure correctly the interface. The deembedded Z11 profile is identical to Z11 profile of the RLC load presented in figure 13-5. You can click on the button “Save” to export the deembedded S11 in a .s1p file, and compare with the S11 simulation of the RLC load.

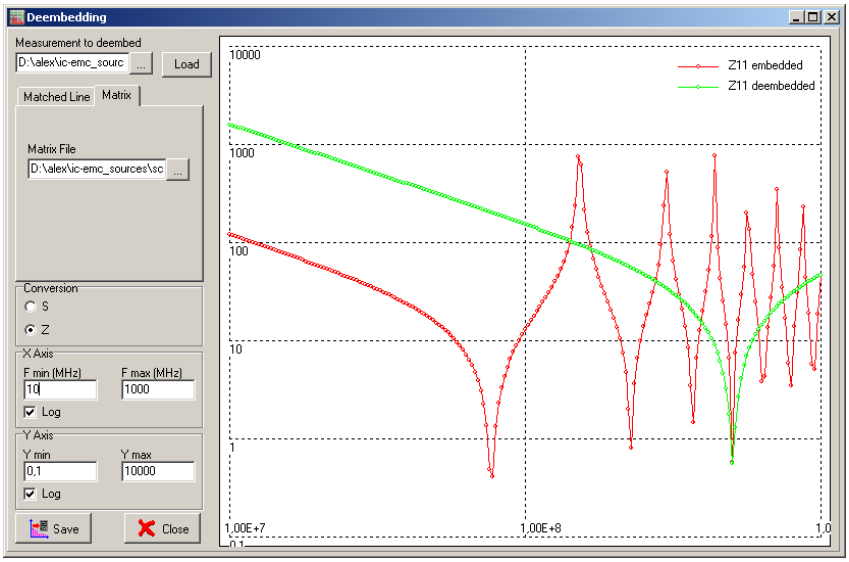


Figure 13-9 : Raw and deembedded S11 measurement (Basic\ deembed\S11_rawDeembed.sch)

14 Appendix D – Non-linear effects in Integrated Circuit

The integrated circuit structures as intrinsically non-linear. The non-linear devices react to sinusoidal waveform and create parasitic offset (also called rectification) or demodulation. As an example, the current through a diode is a function of the voltage which may be written using a general equation 14-1. The H0 and H1 coefficient characterize the linear dependence between the voltage *v* and the current *i*. The non-linear effects are introduced by coefficients H2, H3, etc… Usually, the non-linearity analysis is limited to coefficient H2.

$$i(t) = H_0 + H_1 v + H_2 v^2 + H_3 v^3 + \ldots \qquad \textit{Equ. 14-1}$$

Considering the I(V) characteristic of a diode, such as the one found in input protection devices in CMOS integrated circuits, the dependence between the current and the voltage is strongly non-linear. The difference between a linear and the measured characteristics are given in figure 14-1. There exists no zone where the diode can be considered as a linear component.

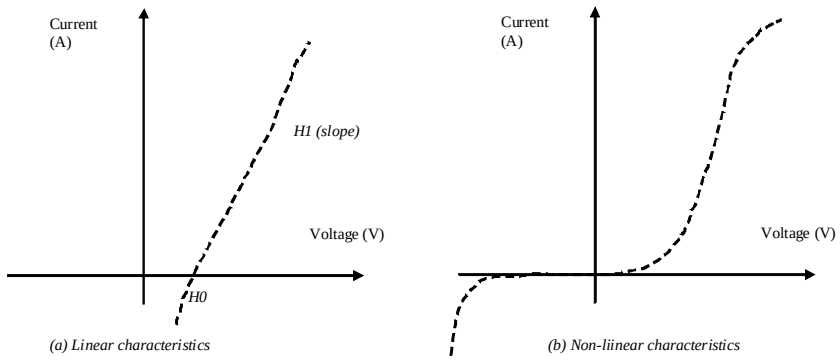


Figure 14-1 : linear vs. non-linear characteristics

If we consider the current as:

$$i(t) = H_0 + H_1 v + H_2 v^2 \qquad \textit{Equ. 14-2}$$

The current in the case of a sinusoidal input is given by equation 14-3. We can see a high frequency component at *2f* and a DC shift.

$$i(t) = H_0 + H_1 \cdot E \cdot \sin(2\pi ft) + \frac{H_2 E^2 [1 + \cos(4\pi ft)]}{2} \qquad \textit{Equ. 14-3}$$

Input waveform		**DC Shift**
Continuous Wave, CW	$E \cdot \sin(2\pi ft)$	$\frac{H_2 \cdot E^2}{2}$
Amplitude modulation	$E \cdot [1 + m \cdot \sin(2\pi f_m t)] \cdot \sin(2\pi ft)$	$\frac{H_2 \cdot E^2}{2} \cdot \left(1 + \frac{m^2}{2}\right)$
Phase modulation	$E \cdot \sin[2\pi ft + \theta \sin(2\pi f_m t)]$	$\frac{H_2 \cdot E^2}{2} \cdot \left(1 + \frac{3 \cdot \theta^4}{2}\right)$

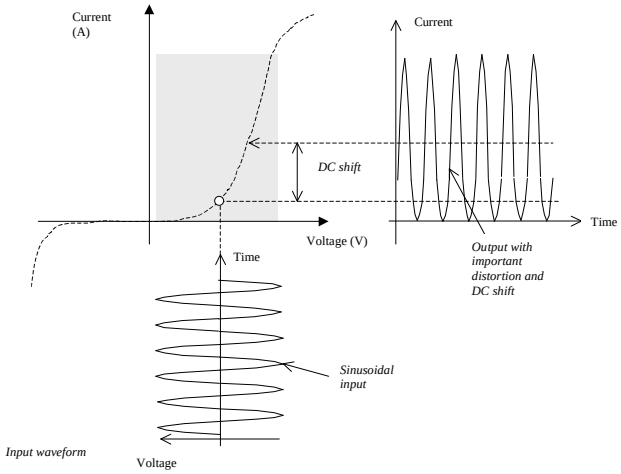


Figure 14-2 : origin of the DC shift due to non linear diode characteristics

15 Appendix E – Threshold voltages – Noise margins

Various standards for IC supply voltages exist, as shown in the table 15-1. The table lists the supply levels and the noise margins associated to different technologies. These elements influence directly the susceptibility of circuits. The smaller is the power supply voltage, the smaller is the noise margin and the immunity to RFI.
The TTL standard works with non-symmetrical low and high levels, as the low voltage TTL (LVTLL) standard. All CMOS standards are almost symmetrical. The illustration of Vin-low,Vin-high, Vout-low and Vout-high is given in figure 15-1, for a 2.5V CMOS technology (LVCMOS2V5).

Standard	VSS (V)	VDD(V)	Vin_low	Vin_high	Vout_low	Vout_high
TTL	0.0	5.0	0.8	2.0	0.4	2.4
LVTTL	0.0	3.3	0.8	2.0	0.4	2.4
LVCMOS2V5	0.0	2.5	0.7	1.7	0.2	2.1
LVCMOS1V8	0.0	1.8	0.63	1.17	0.45	1.35
LVCMOS1V2	0.0	1.2	0.43	0.78	0.30	0.9
LVCMOS1V0	0.0	1.0	0.35	0.65	0.25	0.75

Table 15-1: The format of some basic I/O standards in TTL and CMOS integrated circuits

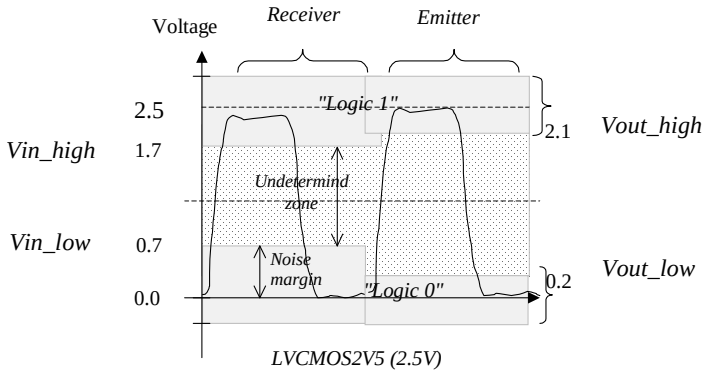


Figure 15-1 : illustration of the voltage specifications for a CMOS 2.5V technology

16 Appendix F: Fourier analysis

The Fourier transform is a powerful mathematical tool to compute the frequency domain representation of a complex signal defined in time domain. IC-EMC proposes a Fast Fourier Transform tool to plot the frequency domain representation of a transient signal. This analysis is required for emission simulation, which are usually done in frequency domain. The Fourier Transform embedded in IC-EMC is controlled by the following parameters:

- Number of points (in time domain)
- Type of Window

16.1 Number of Points

IC-EMC calculates the development in Fourier series of the time domain samples, to extract their frequency contents. The mathematical base of the time/frequency transformation is the formula presented in Eq. 16-1 which describes any function x(t) with a period T, as an infinite sum of cosine and sine of frequencies multiple of a fundamental frequency (Equ. 16-2 and 16-3).

$$x(t) = \sum_{n=0}^{\infty} (a_n \cos 2\pi n \frac{t}{T} + b_n \sin 2\pi n \frac{t}{T}) \quad \textit{Equ. 16-1}$$

where

$$a_n = \frac{2}{T} \int_0^T x(t) \cos(2\pi n \frac{t}{T}) dt \quad \textit{Equ. 16-2}$$

$$b_n = \frac{2}{T} \int_0^T x(t) \sin(2\pi n \frac{t}{T}) dt \quad \textit{Equ. 16-3}$$

$$C_n = \sqrt{a_n^2 + b_n^2} \quad \textit{Equ. 16-4}$$

$$V_{dBuV} = 20.\log\left(C_n x 10^6\right) \quad \textit{Equ. 16-5}$$

The information plotted in the FFT window is V_{dBuV} expressed by Equ. 16-5, corresponding to the module of a_n and b_n, in dBµV unit.
The FFT algorithm implemented in the tool IC-EMC works on a number of samples for x(t), that should be equal to the power of 2 of an integer. When reading a simulation file, IC-EMC converts the time-varying step into a fixed step (0.1 ns). Then, the FFT is adapted to the number of available samples.

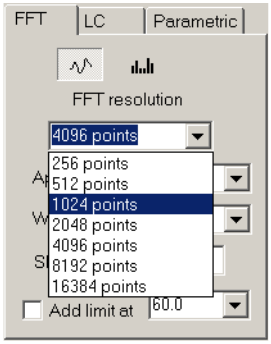


Figure 16-1 : The FFT is always applied to 2^n samples

In IC-EMC, the FFT is performed on 2^n points, where n=8 to 14. The value of *n* is adjusted to the number of information contained in the simulation the following way:

- The initial 10 ns are skipped to ignore the transient part of the signal affected by initial conditions, as illustrated in figure 16-2. This parameter is user-accessible in the menu.
- IC-EMC extrapolates the SPICE curve in order to load one point each 100 ps. This fixed time step enables a valid frequency conversion up to 5 GHz.
- IC-EMC computes the highest value of *n* for which 2^n is less that the number of points stored. For example, if the number of extrapolated points is 10000, the nearest value of n is 13 (2^{13}= 8192).

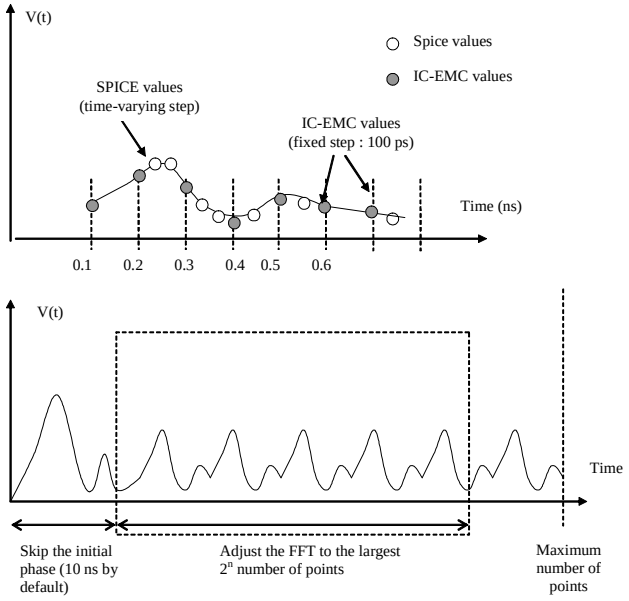


Figure 16-2 : From time-domain to frequency domain

16.2 Windowing

The Windowing is a pre-processing of original data to reduce the numerical noise. Three windows are considered: the rectangular window, the Blackman and the hamming window. The best result is usually obtained with the Blackman window, which limits the numerical noise. See part 3.2 Fourier Transform to have more details about theory of Fourier transform and effects of windowing.

```
rectangular[i] := 1.0;
blackman[i] := 0.42-0.5*cos(2*pi*i/n)+0.08*cos(4*pi*i/n);
hamming[i] := 0.54-0.46*cos(2*pi*i/n);
```

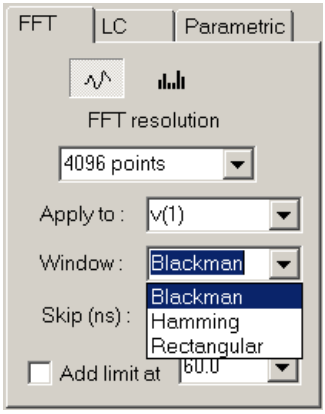


Figure 16-3 : Fast Fourier Transform windowing

17 Appendix G: Interconnect parameter formulations

The tool Interconnect Parameter is dedicated to the evaluation of parasitic R, L, C of different types of usual interconnects, and the automatic generation of SPICE equivalent model. This appendix provides details about the formulations used to compute the electrical parasitics of these interconnects. Table 17-1 lists the interconnection types supported by IC-EMC.

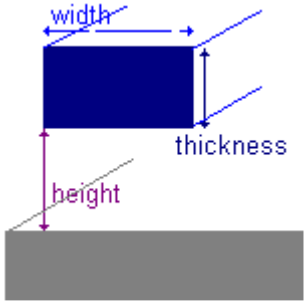
	Microstrip line
	Centered stripline
	Burried microstrip line
	Edge coupled microstrip line
	Edge coupled stripline
	Loop antenna
	Cylindrical via
	Coplanar waveguide
	Coplanar waveguide above ground
	N parallel microstrip lines

Table 17-1: Interconnect cross section supported by IC-EMC

17.1 Microstrip line formulations

17.1.1 Microstrip line

Formulations used to compute L and C of microstrip lines are based on Hamerstad formulations [17-1]. Formulations assume that conductor cross sections are circular.



w : conductor width
t : conductor thickness
h: height of the conductor above ground
μ_0: magnetic permeability = $4\pi\times10^{-7}$
ε_0 : electric permittivity = 8.85 e $^{-12}$ F/m

tan δ: loss tangent (dielectric loss)

Figure 17-1 : Microstrip line

Inductance:

$$L_{11}(H/m) = \frac{\mu}{2\pi}\ln\left(\frac{8h}{w}+\frac{w}{4h}\right) \qquad \textit{Equ. 17-1}$$

Capacitance:

The capacitance is given by equations 17-2 and 17-3.

$$C_{11}(F/m) = \frac{2\pi\varepsilon_0\varepsilon_{eff}}{\ln\left(\frac{8h}{w} + \frac{w}{4h}\right)} \qquad \textit{Equ. 17-2}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 10\frac{h}{w}\right)^{-\frac{1}{2}} \qquad \textit{Equ. 17-3}$$

Resistance

The resistance is approximated from the cross-section and the conductor resistivity. Copper (Cu), Aluminum (Al) and gold (Au) may be selected. Several dielectrics are also listed and have a significant influence on the results. The skin effect occurs at high frequencies, and increases the resistance of the conductor. This is why the AC resistance (RAC) dominates at 1 GHz (31 mΩ/mm instead of 5mΩ DC).

Symbol	Description	Used for	Resistivity at 25°C
ρ_{cu}	Copper resistivity	Signal transport	1.72 10^{-6}Ω.cm
ρ_{al}	Aluminum resistivity	Signal transport	2.77 10^{-6}Ω.cm
ρ_{Ag}	Gold resistivity	Bonding between chip and package	2.20 10^{-6} Ω.cm
$\rho_{tungsten}$	Tungsten resistivity	Contacts	5.30 10^{-6} Ω.cm
ρ_{Ndiff}	Highly doped silicon resistivity	N+ diffusions	0.25 Ω.cm
ρ_{Nwell}	Lightly doped silicon resistivity	N well	50 Ω.cm
ρ_{si}	Intrinsic silicon resistivity	Substrate	2.5 10^{5} Ω.cm

Table 17-2: Typical material resistivity

IC-EMC computes the DC resistor, which depends on the interconnect cross section and material resistivity.

$$R_{DC}(\Omega/m) = \rho\frac{l}{w.t} \qquad \textit{Equ. 17-4}$$

where
R=serial resistance (ohm)
ρ=resistivity (ohm.m)
w= conductor width (m)
t= conductor thickness (m)
l = conductor length (m)
d = conductor distance (m)

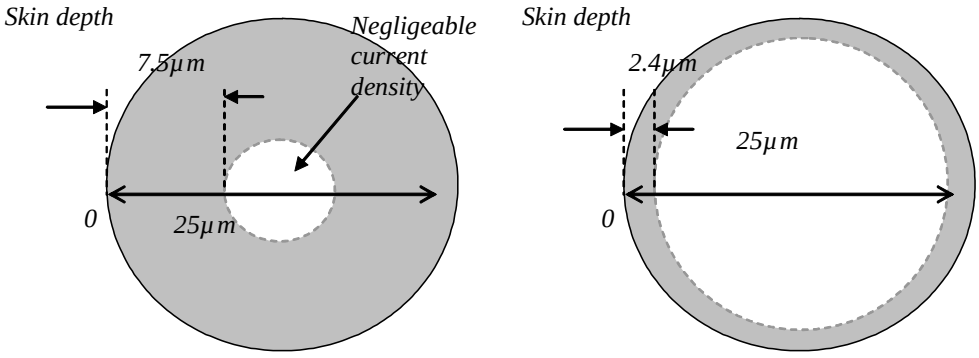
The skin depth is expressed by Equation 3-10. It also appears in the “Resistance” section as illustrated in Fig. 17-2.

$$\delta = \sqrt{\frac{2}{2\pi f\mu_0\gamma}} \qquad \textit{Equ. 17-5}$$

where
f is the signal frequency (Hz)

μ_0 = 1.257e^{-10} H/m, permittivity of vaccum
γ = conductivity (58.0 10^6 S/m for copper, 45.5 10^6 S/m for gold)

At 100 MHz, the skin depth of a gold bonding is 7.5µm, meaning that the current flows in almost the all the conductor section. At 1 GHz the skin depth is 2.4 µm, meaning that the current is flowing only in a reduced section of the conductor, thus increasing significantly its equivalent resistance. More details about the skin effect are given in Appendix C.



Bonding current density at 100 MHz

Bonding current density at 1GHz

Figure 17-2 : bonding current density versus frequency

Characteristic impedance Zo

$$Z_0(\Omega) = \sqrt{\frac{L_{11}}{C_{11}}} \qquad \textit{Equ. 17-6}$$

Propagation delay Tpd

$$T_{PD}(s/m) = \frac{1}{\sqrt{L_{11}C_{11}}} \qquad \textit{Equ. 17-7}$$

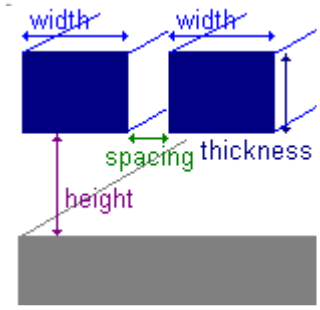
Loss conductance

The loss conductance G is associated to the dielectric losses. This conductance is usually small so that it is not included by default in the generated SPICE model. Equation 17-7 gives a formulation to compute the loss conductance per unit length [17-2].

$$G(S/m) = \omega \tan\delta \times C_{11} \qquad \textit{Equ. 17-8}$$

17.1.2 Edge coupled microstrip line

Formulations used to compute L and C of edge coupled microstrip lines are based on Delorme formulations [17-1]. Formulations assume that conductor cross sections are circular.



w : conductor width
t : conductor thickness
h: height of the conductor above ground
s: spacing between the conductors
μ_0: magnetic permeability = $4\pi\times10^{-7}$
ε_0 : electric permittivity = 8.85 e $^{-12}$ F/m

tan δ: loss tangent (dielectric loss)

Figure 17-3 : Edge coupled microstrip line

Self inductance

$$L_{11}(H/m) = \frac{\mu_0}{2\pi}.\ln\left(\frac{2h}{r}+1\right) \quad \textit{Equ. 17-9}$$

with r the equivalent radius:

$$r = \frac{t+w}{4}$$

Mutual inductance

$$L_{12}(H/m) = \frac{\mu_0}{2\pi}.\ln\left(\frac{(s+2r)^2+(r+2H)^2}{(s+2r)^2+r^2}\right. \quad \textit{Equ. 17-10}$$

Self capacitance

$$C_{11}(F/m) = \varepsilon_0\varepsilon_r\left(1.11\frac{w}{h}+0.79\left(\frac{w}{h}\right)^{0.1}+0.59\left(\frac{t}{h}\right)^{0.53}+\left(0.52\left(\frac{w}{h}\right)^{0.01}+0.46\left(\frac{t}{h}\right)^{0.17}\right)\left(1-0.87e^{-\frac{S}{h}}\right)\right)$$

Equ. 17-11

Mutual capacitance

$$C_{12}(F/m) = \varepsilon_0\varepsilon_r\left(\frac{t}{s}+1.21\left(\frac{t}{h}\right)^{0.1}\left(\frac{s}{h}+1.15\right)^{-2,22}+0.25\ln\left(1+7.17\frac{w}{s}\right)\left(\frac{s}{h}+0.54\right)^{-0.64}\right)$$

Equ. 17-12

17.1.3 N parallel microstrip lines

A PEEC method is used to extract self and mutual inductances of capacitances of the interconnects (see appendix H). The interconnects can have various dimensions, they can be or not above a perfect ground plane. In IC-EMC, the number of interconnects is limited to 8. The extraction of L and C is based on a numerical solving method so that it takes several seconds to provide results.

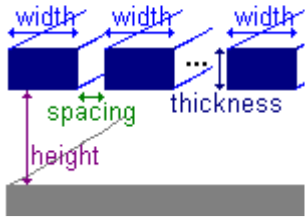


Figure 17-4 : N parallel microstrip lines

N: number of interconnects
w : conductor width
t : conductor thickness
h: height of the conductor above ground
s: spacing between the conductors
μ_0: magnetic permeability = $4\pi\times10^{-7}$
ε_0 : electric permittivity = 8.85 e $^{-12}$ F/m

tan δ: loss tangent (dielectric loss)

17.1.4 Buried microstrip line

A buried microstrip line is a microstrip embedded in a substrate. Formulations for this type of conductor are given in [17-3].

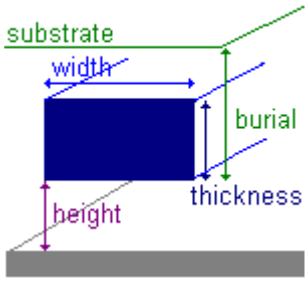


Figure 17-5 : Burried microstrip line

w : conductor width
t : conductor thickness
h: height of the conductor above ground
b: burial depth of the conductor
μ_0: magnetic permeability = $4\pi\times10^{-7}$
ε_0 : electric permittivity = 8.85 e $^{-12}$ F/m

tan δ: loss tangent (dielectric loss)

Characteristic impedance of a buried microstrip line

$$Z_0(\Omega) = Z_{0\,microstrip}\sqrt{\frac{\varepsilon_{eff\ microstrip}}{\varepsilon_{eff\ buried}}} \qquad \textit{Equ. 17-13}$$

where

$Z_{0\ microstrip}$ is the characteristic impedance of a non buried microstrip line
$\varepsilon_{eff\ microstrip}$ is the effective relative constant of a non buried microstrip line
$\varepsilon_{eff\ buried}$ is the effective relative constant of a buried microstrip line

$$\varepsilon_{eff\ buried} = \varepsilon_{eff}\, e^{-\frac{2b}{h}} + \varepsilon_r\left(1 - e^{-\frac{2b}{h}}\right) \qquad \textit{Equ. 17-14}$$

Characteristic impedance of a microstrip line

$$Z_{0\,microstrip} = \frac{377}{2\sqrt{2}\pi\sqrt{\varepsilon_r + 1}}\ln\left[1 + \frac{4h}{w_{eff}}\left(\frac{14+\frac{8}{\varepsilon_r}}{11}\frac{4h}{w_{eff}} + \sqrt{\left(\frac{14+\frac{8}{\varepsilon_r}}{11}\right)^2\left(\frac{4h}{w_{eff}}\right)^2 + \frac{1+\frac{1}{\varepsilon_r}}{2}\pi^2}\right)\right] \qquad \textit{Equ. 17-15}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + \frac{12h}{w}\right)^{-0.5} + 0.04\left(1 - \frac{w}{h}\right)^2\right] \quad if\ \frac{w}{h} \le 1$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{w}\right)^{-0.5} \quad if\ \frac{w}{h} > 1 \qquad \textit{Equ. 17-16}$$

These formulations are valid (1% error) if $\varepsilon_r < 16$, $0.05 \le \frac{w}{h} \le 20$.

$$w_{eff} = w + \Delta w' \qquad \textit{Equ. 17-17}$$

$$\Delta w' = \Delta w\left(\frac{1 + \frac{1}{\varepsilon_r}}{2}\right) \qquad \textit{Equ. 17-18}$$

$$\Delta w = \frac{t}{\pi}\ln\left(\frac{4e}{\sqrt{\left(\frac{t}{h}\right)^2 + \left(\frac{\frac{1}{\pi}}{\frac{w}{t} + 1.1}\right)^2}}\right) \qquad \textit{Equ. 17-19}$$

Propagation speed

$$v_P(m/s) = \frac{1}{\sqrt{\mu_0 \mu_r \varepsilon_0 \varepsilon_{eff}}} \qquad \textit{Equ. 17-20}$$

Inductance

$$L_{11}(H/m) = \frac{Z_0}{v_P} \qquad \textit{Equ. 17-21}$$

Capacitance

$$C_{11}(F/m) = \frac{1}{Z_0 v_P} \qquad \textit{Equ. 17-22}$$

17.2 Loop antenna

The formulations are described in section 12.8.

17.3 Cylindrical via

A via connect two metallic interconnections separated by a dielectric layer. The via is mainly inductive and resistive. Its parasitic capacitance is neglected.

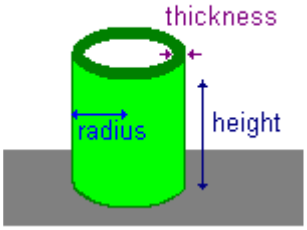


Figure 17-6 : Cylindrical via

r : via radius
t : conductor thickness
h: via height or separation between metal layers
μ_0: magnetic permeability = $4\pi\times10^{-7}$
tan δ: loss tangent (dielectric loss)

Inductance:

$$L_{11}(H/m)=\frac{\mu_0}{2\pi}\left(h\ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right)+1.5\left(r-\sqrt{r^2+h^2}\right)\right) \quad \textit{Equ. 17-23}$$

Resistance

$$R_{DC}(\Omega/m)=\rho\frac{l}{2\pi\, r.t} \qquad \textit{Equ. 17-24}$$

17.4 Coplanar waveguide

17.4.1 Coplanar waveguide

A coplanar waveguide is a conductor surrounded by ground plane on the same layer, that ensure the return of current. No ground plane is present below the line. Formulations for coplanar waveguides are given in [17-3].

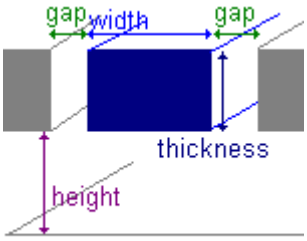


Figure 17-7 : Coplanar waveguide

w : conductor width
t : conductor thickness
h: thickness of the substrate
g: gap between the conductor and the coplanar ground plane
b = w+2g
μ_0: magnetic permeability = $4\pi\times10^{-7}$
ε_0 : electric permittivity = 8.85 e $^{-12}$ F/m
tan δ: loss tangent (dielectric loss)

Characteristic impedance

$$Z_0(\Omega)=\frac{30\pi}{\sqrt{\varepsilon_{eff,t}}}\frac{K(k_t')}{K(k_t)} \qquad \textit{Equ. 17-25}$$

with :

$$\varepsilon_{eff,t}=\varepsilon_{eff}-\frac{\varepsilon_{eff}-1}{\frac{b-w}{1.4t}\frac{K(k')}{K(k)}+1} \qquad \textit{Equ. 17-26}$$

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')} \qquad \textit{Equ. 17-27}$$

$$k_t = \frac{w_t}{b_t} \qquad \textit{Equ. 17-28} \qquad\qquad k = \frac{w}{b} \qquad \textit{Equ. 17-29}$$

$$k_t' = \sqrt{1 - k_t^2} \qquad \textit{Equ. 17-30} \qquad\qquad k' = \sqrt{1 - k^2} \qquad \textit{Equ. 17-31}$$

$$k_1 = \frac{\sinh\left(\frac{\pi w_t}{4h}\right)}{\sinh\left(\frac{\pi b_t}{4h}\right)} \qquad \textit{Equ. 17-32} \qquad k_1' = \sqrt{1 - k_1^2} \qquad \textit{Equ. 17-33}$$

$$w_t = w + \frac{1.25t}{\pi}\left(1 + \ln\left(\frac{4\pi w}{t}\right)\right) \qquad \textit{Equ. 17-34} \qquad b_t = b - \frac{1.25t}{\pi}\left(1 + \ln\left(\frac{4\pi b}{t}\right)\right) \qquad \textit{Equ. 17-35}$$

$\frac{K(k')}{K(k)}$ is the ratio of complete elliptic integrals of the first kind [17-4].

$$\frac{K(k')}{K(k)} = \frac{1}{2\pi} \ln\left(2\frac{\sqrt{1+k} + \sqrt[4]{4k}}{\sqrt{1+k} - \sqrt[4]{4k}}\right) \qquad \textit{Equ. 17-36} \qquad \textit{si } \frac{1}{\sqrt{2}} \le k \le 1$$

$$\frac{K(k')}{K(k)} = \frac{2\pi}{\ln\left(2\frac{\sqrt{1+k} + \sqrt[4]{4k}}{\sqrt{1+k} - \sqrt[4]{4k}}\right)} \qquad \textit{Equ. 17-37} \qquad \textit{si } 0 \le k \le \frac{1}{\sqrt{2}}$$

Propagation speed

$$v_P(m/s) = \frac{1}{\sqrt{\mu_0 \mu_r \varepsilon_0 \varepsilon_{eff}}} \qquad \textit{Equ. 17-38}$$

Inductance

$$L_{11}(H/m) = \frac{Z_0}{v_P} \qquad \textit{Equ. 17-39}$$

Capacitance

$$C_{11}(F/m) = \frac{1}{Z_0 v_P} \qquad \textit{Equ. 17-40}$$

17.4.2 Coplanar waveguide with ground

A coplanar waveguide is a conductor surrounded by ground plane on the same layer and a ground plane on the bottom side. These different planes ensure the return of current. Formulations for coplanar waveguides are given in [17-3]. The formulations are very similar to those of the coplanar waveguide. Only formulations with some differences are detailed.

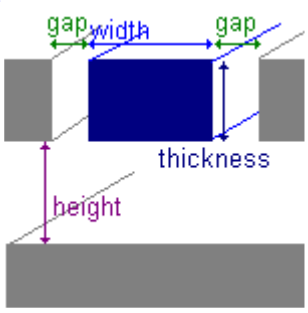


Figure 17-8 : Coplanar waveguide with ground

w : conductor width
t : conductor thickness
h: height of the conductor above ground
g: gap between the conductor and the coplanar ground plane
b = w+2g
μ_0: magnetic permeability = $4\pi\times10^{-7}$
ε_0 : electric permittivity = 8.85 e $^{-12}$ F/m

tan δ: loss tangent (dielectric loss)

Characteristic impedance

$$Z_0(\Omega) = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{\frac{K(k')}{K(k)} + \frac{K(k_1)}{K(k_1')}} \qquad \textit{Equ. 17-41}$$

$$k_1 = \frac{\tanh\left(\frac{\pi w}{4h}\right)}{\tanh\left(\frac{\pi b}{4h}\right)} \qquad \textit{Equ. 17-42}$$

$$\varepsilon_{eff} = \frac{1+\varepsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1+\frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}} \qquad \textit{Equ. 17-43}$$

17.5 References

[17-1] Hammerstadt E. O., O. Jensen, “Accurate Models for Microstrip Computer-Aided Design”, 1980 IEEE MTT-S International Microwave Symposium Digest, pp. 407-409

[17-2] C. R. Paul, “Analysis of Multiconductor Transmission Lines”, Wiley Interscience, 1994, ISBN 0-471-02080

[17-3] B. C. Wadell, “Transmission Line Design Handbook”, Artech House, 1991, ISBN 0-89006-436-9

[17-4] W. Hilberg, “From Approximations to exact Relations for Characteristic Impedances”, IEEE Transactions on Microwave Theory and Techniques, Vol. MTT 17, No 5, May 1969, pp. 259-265.

18 Appendix H: Package model extraction by PEEC method

Parasitic electrical elements of package influence directly the voltage bounce in an IC, especially inductances. It has also an influence on emission and susceptibility. Therefore, electrical model of IC packages is a major element in an EMC model. Due to the small size of package, a R, L, C model of a package is valid up to several GHz.
In chapter 4 about IBIS, a fast method for package model extraction based on simple geometrical information was presented. This method is adapted for a simple evaluation of package model, but the computed values are not accurate because the geometrical model is an approximation. In order to produce more accurate package model, a second method is implemented under IC-EMC. This method is based on a more realistic geometrical model construction followed by a R, L, C extraction based on a Partial Element Equivalent Circuit (PEEC) algorithm [18-1].
The PEEC method is a popular electromagnetic solving method adapted to coupling problems in electronic devices (cables, boards, circuits). This method is able to extract an equivalent passive circuit from an electromagnetic problem, so that electrical network simulators as SPICE can be used to solve problems.

18.1 Partial element theory

Any electrical conductor can be represented by an electrical model in order to predict the evolution of signals along the conductor. The simplest model is a model with localized R, L, C. This type of model is frequency limited because the notion of localized constant is based on the quasi-static approximation. Though, the valid frequency range can be extent when the number of localized R, L, C are increased or distributed along the conductor. Couplings between nearby conductors can also be modeled by electrical model. An electric field coupling can be modeled by an equivalent capacitor while a magnetic field coupling can be modeled by an equivalent inductor. The values of electrical elements can be extracted by analytical formulation as those used in "Tools → Interconnect Parameters" [18-2] [18-3]. However, these methods are limited to simple geometry. For complex geometry, a numeric solving method like PEEC applied on 3D geometrical models is more adapted.
PEEC is based on the concept of partial elements, where each small elements of a conductor can be modeled by a partial element (a resistance, a self or mutual inductor, a capacitor or a mutual capacitor) that contributes to the total impedance of the conductor. Figure 18-1 illustrates the concept of partial elements on a rectangular loop. Each side of the loop is decomposed in a partial resistance and inductance. Each partial self inductor of the loop are coupled with the other inductor by a mutual inductor.

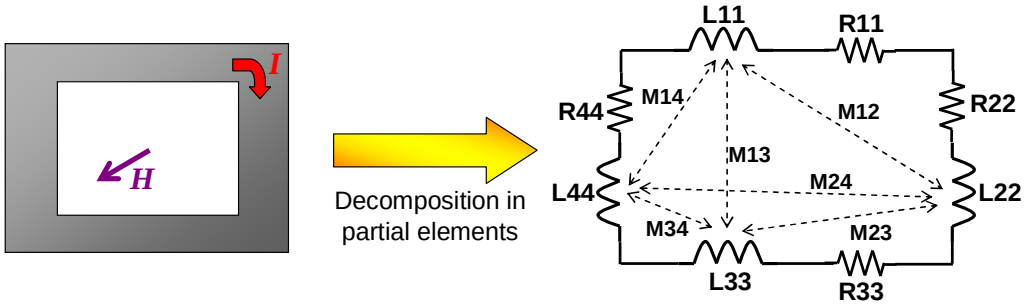


Figure 18-1 : Decomposition in partial elements of a rectangular loop [18-4]

Knowing the values of partial elements, the total resistance and inductance of the loop can be computed using equations 18-1 et 18-2. The total resistance is linked to the circulation of current along each partial element. The total inductance is linked to the flux of magnetic field through the loop surface so that it is equal to the sum of every self and mutual partial inductor.

$$R_{tot} = \sum_i R_{ii} \qquad \textit{Equ. 18-1}$$

$$L_{tot} = \sum_i L_{ii} + \sum_i \sum_j M_{ij} \qquad \textit{Equ. 18-2}$$

18.2 PEEC method

The PEEC method was developed in 1972 by A. Ruehli [18-1] to analyze electrical interconnects with complex and arbitrary shapes. The principle is the conversion of each of physical structures (track, plane, substrate, via…) into equivalent passive model with localized R, L, C. Figure 18-2 illustrates the PEEC methodology to build an equivalent model from a geometrical model.

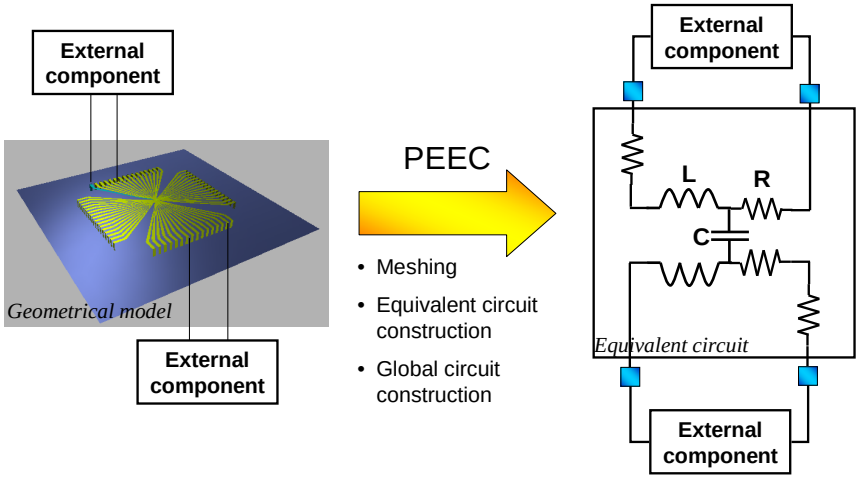


Figure 18-2 : PEEC method description

PEEC method is not a full wave or exact electromagnetic method because it is based on the quasi-static approximation. This approximation simplifies the resolution of Maxwell equations by assuming that wave propagation speed is infinite in a structure with a given length. Therefore, the structure is supposed to be an equipotential.

The PEEC method is based on the Electrical Field Integral Equation (EFIE) solving, presented in equation 18-3. The total electric field is equal to the contribution of incident field Ei and scattering field Es induced by currents and charges on the structure.

$$\vec{E}_{tot} = \vec{E}_i + \vec{E}_s \qquad \textit{Equ. 18-3}$$

From this equation, an equivalent passive circuit can be extracted with resistive, inductive and capacitive contributions. For each partial elements of the studied structure, the incident field is supposed to be null. The scattering electric field can be expressed with scalar and potential vectors as shown in equation 18-4.

$$\vec{E}_{tot} = -\frac{\partial}{\partial t}\vec{A} - \vec{\nabla}V \qquad \textit{Equ. 18-4}$$

Expressions of potentials are respected and equation 18-5 is obtained. The total field induced by current and charges present at a point r' can be computed at any point r.

$$\vec{E}_{tot}(r,t) = -\frac{\partial}{\partial t}\left[\frac{\mu_r \mu_o}{4\pi}\int_V \frac{1}{|r-r'|}\vec{J}(r')dV\right] - \vec{\nabla}\left[\frac{1}{4\pi\varepsilon_o\varepsilon_r}\int_S \frac{1}{|r-r'|}q(r')dS\right] \qquad \textit{Equ. 18-5}$$

The PEEC method is a numeric method so that the geometrical structure must be meshed in N

elementary cells characterized by a volume Vi, a section Ai and lateral section Si. Equation 18-5 can be rewritten in the following form:

$$\vec{E}_{tot}(r,t)+\sum_{i=1}^{N}\left[\frac{\mu_r\mu_o}{4\pi A_i}\frac{\partial I_i}{\partial t}\int_{Vi}\frac{1}{|r-r'|}dV_i\right]+\sum_{i=1}^{N}\left[\frac{1}{4\pi\varepsilon_o\varepsilon_r S_i}\vec{\nabla}q_i\int_{Si}\frac{1}{|r-r'|}dS_i\right]=\vec{0} \qquad \textit{Equ. 18-6}$$

In order to determine the electromagnetic behavior of an elementary cell, the electric field is averaged on all the cell section with the following operator: $\frac{1}{A_j}\int_{Vj}dV_j$.

Finally equation 18-7 can be written:

$$\frac{1}{A_j}\int_{Vj}\vec{E}_{tot}(r,t)+\sum_{i=1}^{N}\left[\frac{\mu_r\mu_o}{4\pi A_i A_j}\frac{\partial I_i}{\partial t}\int_{Vj}\int_{Vi}\frac{1}{|r-r'|}dV_i dV_j\right]+\sum_{i=1}^{N}\left[\frac{1}{4\pi\varepsilon_o\varepsilon_r S_i S_j}\vec{\nabla}q_i\int_{Sj}\int_{Si}\frac{1}{|r-r'|}dS_i dS_j\right]=\vec{0} \quad \textit{Equ. 18-7}$$

The first term is the resistive contribution or the self resistor of the meshed partial element. The second term is the inductive contribution, containing the self inductance of the partial element and all the mutual inductances with other partial elements. The last term is the capacitive contribution, containing the potential of the partial element and the potential compared to the other partial elements. This equation is applied to every partial elements of the meshed structure which can be replaced by equivalent R, L, C circuits.
When the previous equation has been solved on each partial element, the complete structure can be modelled by an equivalent electrical circuit that can be solved with an electrical solver as SPICE.

18.3 Application to rectangular section conductors

The figure 18-3 illustrates the meshing of two conductor adapted to the partial inductance computation [18-5]. Each conductor is meshed in elementary cell along all its length, so that the current can flow through an elementary volume.

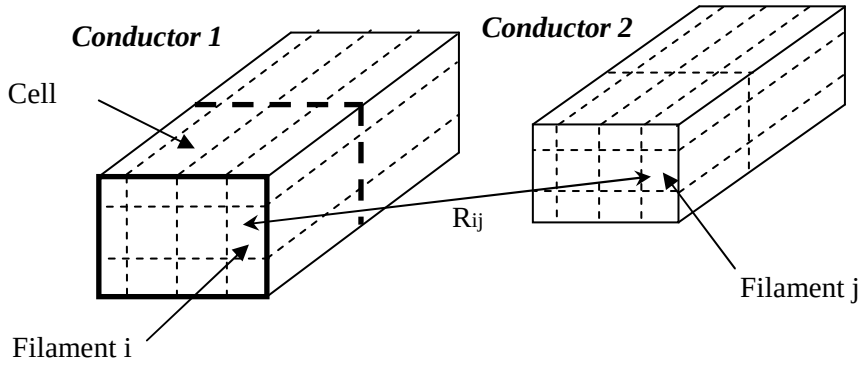


Figure 18-3 : Meshing in elementary filaments of two conductors

From equation 18-7, the inductive contribution can be isolated as described by equation 18-8.

$$L_{12}=\frac{\mu_o}{4\pi A_1 A_2}\int_{cond\ 1}\int_{cond\ 2}\frac{l_1\times l_2}{|r_1-r_2|}dV_2 dV_1 \qquad \textit{Equ. 18-8}$$

- L_{12} : partial inductance between conductors 1 and 2
- A_1, A_2 : section of conductors 1 and 2
- li, lj: orientation of filament i and j
- R_{ij} : distance between meshes i and j

- dV_i, dV_j : elementary volumes between meshes i and j

The result of partial inductance extraction by PEEC method is given in the form of a partial inductance matrix. Self inductances are present in the diagonal of the matrix.
The figure 18-4 illustrates the meshing of two conductors dedicated to the partial capacitor computation. Each meshed conductor is meshed along all its length in elementary cells. The lateral surface is meshed in elementary panels on which the total charge is spread.

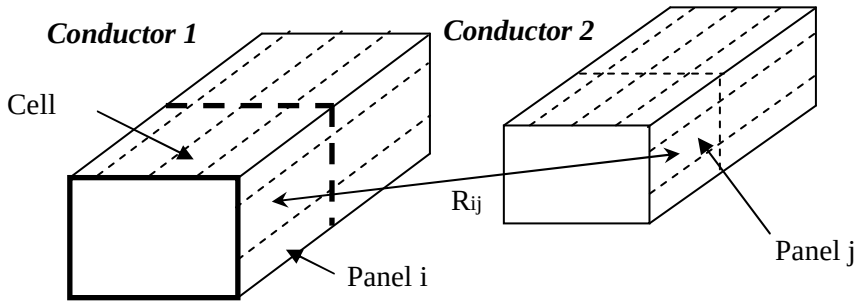


Figure 18-4 : Meshing in elementary panels of two conductors

From equation 18-7, the capacitive contribution can be isolated. However the expression does not directly give the partial capacitors but provides surface potential as described in equation 18-9.

$$P_{12} = \frac{1}{4\pi\varepsilon S_1 S_2}\int_{cond\,1}\int_{cond\,2}\frac{1}{|r_1 - r_2|}dA_2 dA_1 \qquad \textit{Equ. 18-9}$$

- P_{12} : potential between conductors 1 and 2
- S_1, S_2 : lateral section of conductors 1 and 2
- R_{ij} : distance between panels i and j
- dA_i, dA_j : elementary surface of panels i and j

The result of equation 18-9 is given in term of a potential matrix P. Capacitor matrix C is obtained by inverting the potential matrix, as shown in equation 18-10.

$$[V] = [P][Q] \quad \Leftrightarrow \quad [C][V] = [Q]$$

$$[C] = [P]^{-1} \qquad \textit{Equ. 18-10}$$

18.4 Implementation in IC-EMC for package model extraction

IC-EMC proposes a tool to build easily realistic geometrical model of package and compute accurately partial inductances, resistances and capacitors. Click “Tools → Advanced Package Model” to open this tool. This tool is composed of 3 parts for the definition of the geometrical model, the visualization of the 3D package geometric model and the computation of partial elements.

18.4.1 Package model construction

When the tool is opened, only the first page called “Package Generation” is visible. This page is dedicated to the construction of the package model. The tool proposed several types of standard package: Dual In Line (DIL), Small Outline Package (SOP), Quad Flat Package (QFP) and Ball Grid Array (BGA). The page is divided in two parts: on the right, numerous geometrical information are

proposed to build geometrical model, reported in figure 18-6.

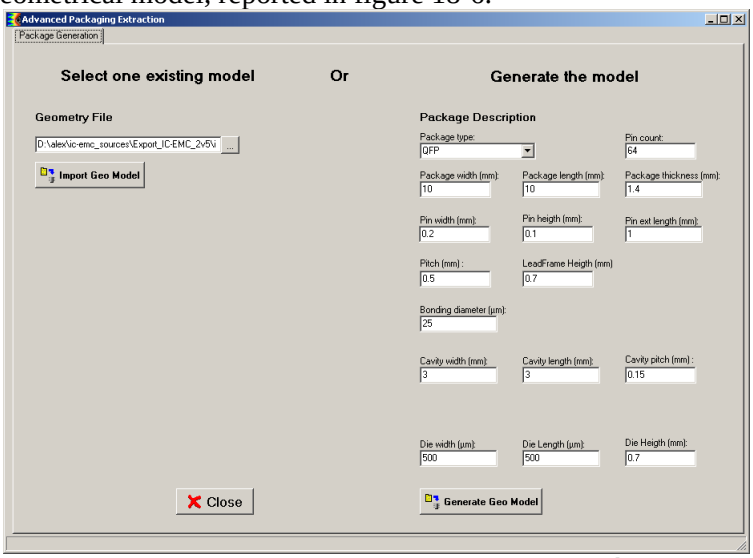


Figure 18-5 : Interface to define realistic package model (Tools → Advanced Package Model)

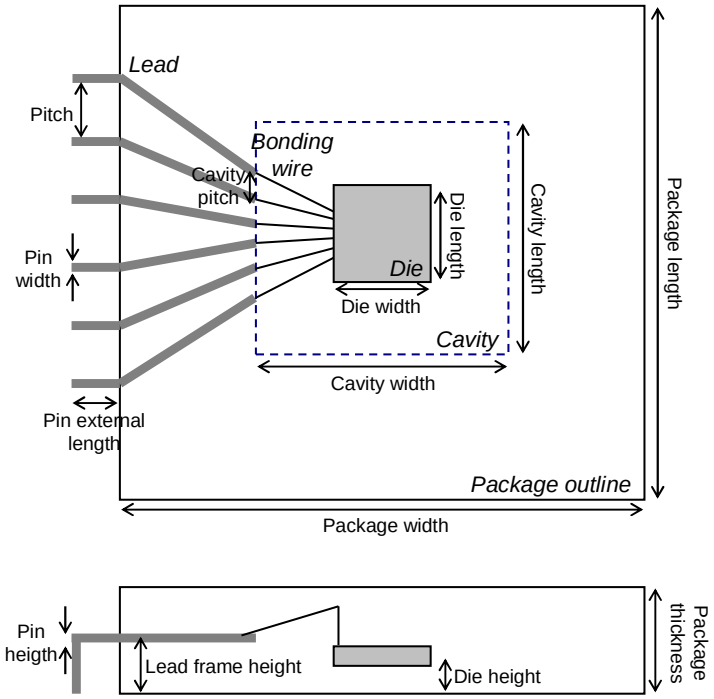


Figure 18-6 : Interface to define realistic package

Click on the button “Generate Geo Model” to build the geometrical model, which is saved in a specific file *.GEO. Only DIL, SOP and QFP are automatically generated. BGA are complex multilayer package and the internal routing can not be automatically reconstructed. If BGA type is selected and you click on Generate Geo Model, a new window is opened to help the user to manually define the internal routing of the BGA.

The left part of the screen is simpler and is dedicated to the import of an existing GEO file previously generated. When the GEO file is correctly imported, the two other pages become visible. Import the file “package\TQFP64.geo” and click on the button “Import Geo Model”. Open the page “Model Viewer” to see the geometrical model of the package (fig. 18-7). The different leads, bonding wires and the die are placed.

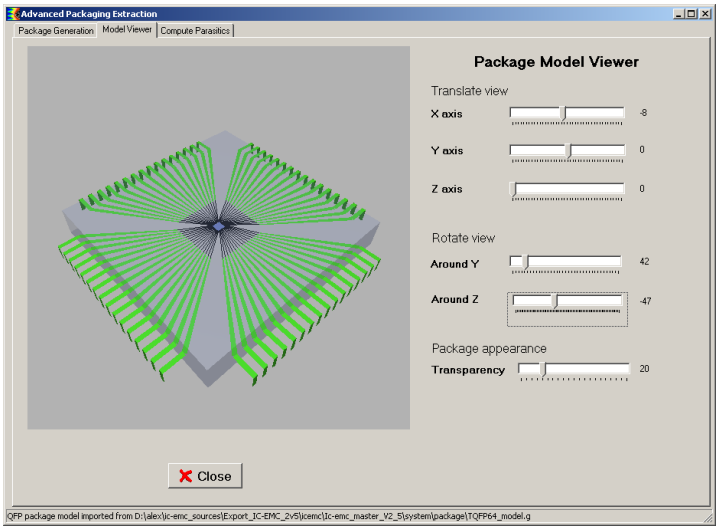


Figure 18-7 : Display of a reconstructed 3D package model of a TQFP 64 (package\TQFP64.geo)

18.4.2 Package partial element extraction

Open the page “Compute Parasitics” to compute the partial elements of package leads and bonding wires. Figure 18-8 presents the screen.

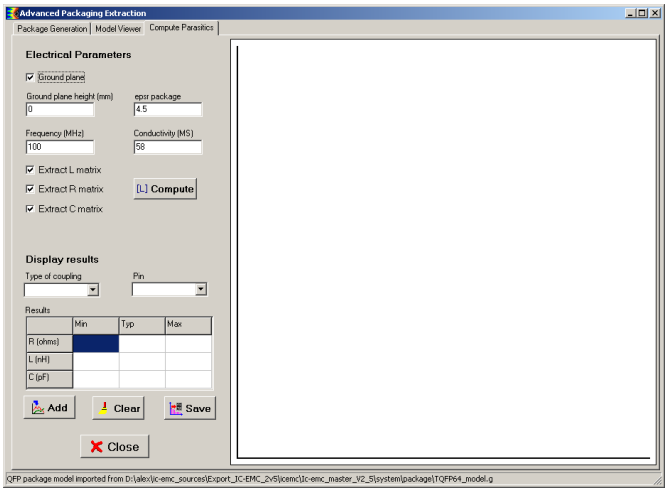


Figure 18-8 : Interface to compute the partial elements of a package

First configure the electrical parameters of the computation. A perfect ground plane is placed under the package. The dielectric constant epsr package of the package is set to 4.5. As the simulator does not take into account dielectric materials, three options are proposed to approximate the effective dielectric constant:

- Free space: the dielectric constant of the space is constant and equal to epsr package
- Microstrip line: the lead are considered as microstrip line, an effective dielectric constant is computed from the height of the substrate, the width of the lead and epsr package
- Burried line: the lead is buried in the substrate, , an effective dielectric constant is computed from the height of the substrate, the width of the lead and epsr package

Set the conductivity of the conductors and the maximum frequency of the computation in order to compute the partial resistance and take into account skin effect. Finally, select the partial element types that you want to compute; R, L or C, and click on the button “Compute”.
The simulation takes several seconds, an advancement bar appears to indicate the advancement of the simulation. At the end of the simulation, the field “Type of Coupling” and “Pin” are filled and you can select the type of partial elements that you want to display. Click on the button Add to display partial

elements for every pins of the package on the graph of the right part of the screen. Figure 18-9 presents the simulated partial self inductance and capacitance for the TQFP64 package.

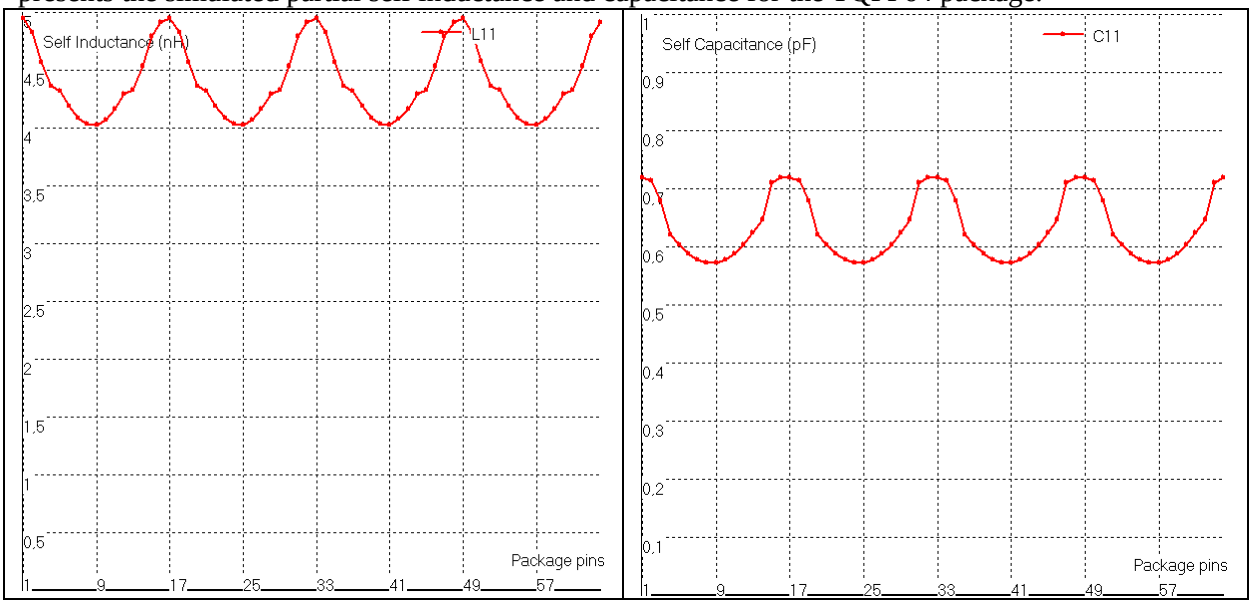


Figure 18-9 : Simulation of the partial self inductance (on the left) and capacitance (on the right) (package\TQFP64.geo)

The different simulated partial elements are exported in .L, .R and .C file for partial inductances, resistances and capacitances respectively.

18.4.3 BGA model construction

BGA geometrical model can not be automatically generated. That's why IC-EMC proposes an interface to help the user to build manually the geometrical model. Return to the first page of the Advanced Package Extraction tool and enter the different mechanical parameters of the package. Click on "Generate Geo Model" to create a new Geo model or "Modify Geo Model" to modify an existing Geo model.

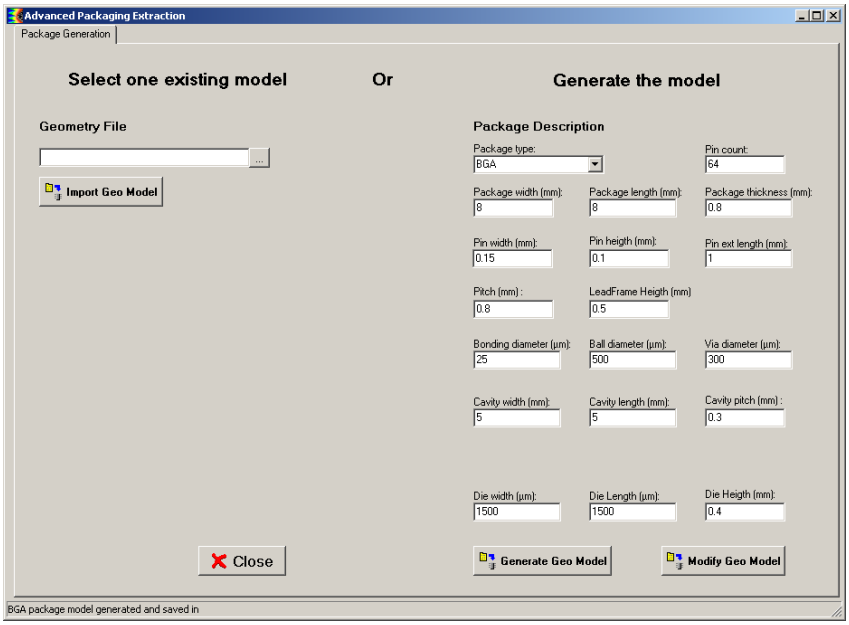


Figure 18-10 : Launch the BGA model manual construction

An open dialog window asks for a .geo file. Then the following screen appears. This screen defines the number of the internal routing layers in the BGA, the characteristics of the tracks for each layer, and

the number and characteristics of embedded dies. Click Add layer to add a new layer and change directly in the tables the different value.

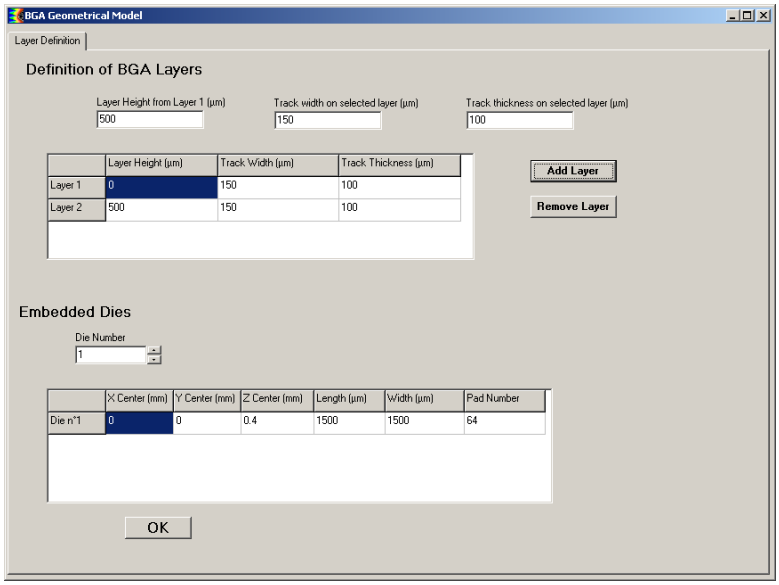


Figure 18-11 : Definition of the BGA internal layers and the number of dies

When the layer and the die information are set, click on the button "OK" to start the manual design of the internal routing of the BGA. A new page called "BGA design" becomes visible, described in figure 18-12 left. The 3D screen is empty, if you change the visible layer to the Layer 2, the die becomes visible. Balls and bonding wires can be accurately automatically placed. Click on the button "Ball Placement", the balls appear on the screen. The button "Bonding Placement" also appears. Click on this button and all the bonding wires are placed, as shown in figure 18-12.

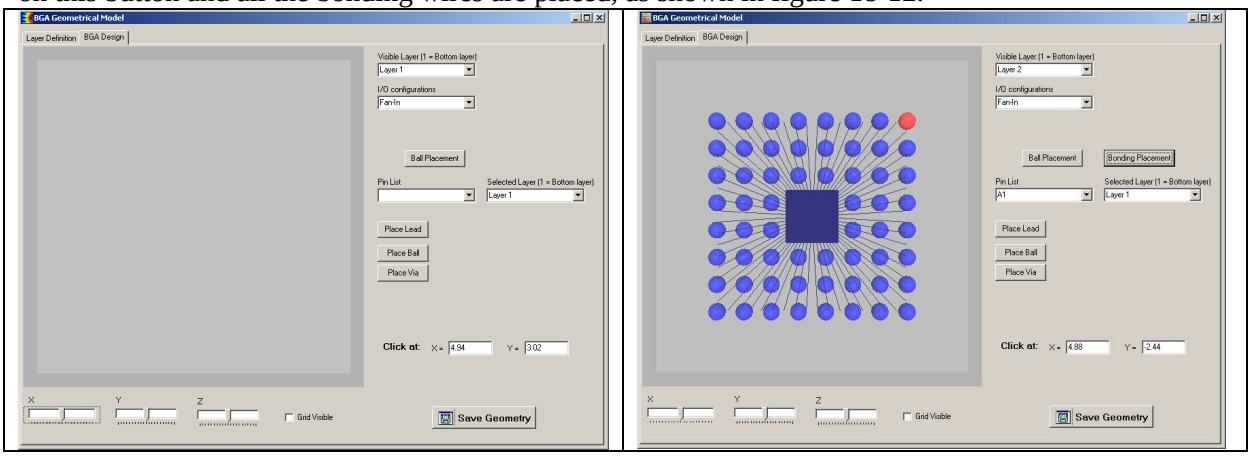


Figure 18-12 : Empty BGA design screen (on the left) and automatic placement of balls and bonding wires (on the right)

The red ball indicates the selected pin from which you can start the pin design. With the field, you can define on which layer you can design a new element of pin design. Three elements can be design: a lead, a ball or a via. Click on one button "Place Lead", "Place Ball" or "Place Via". Push the left button of the mouse to place the first point of the new element (e.g. a lead) and release the mouse to indicate the last point of this element. A yellow shape indicates the new elements. Finally, click on the button "Validate" to confirm the placement of a new element.
Let's design the pin number 1 starting from the ball. Select A1 in "Pin List" field and Layer 1 in "Selected Layer". Place a lead on the first layer. Then place a 300 µm wide via between first and second layers. Finally, place a lead on the second layer that connects the extremity of a bonding wire. The connected bonding wire becomes red, indicated that this bonding wire is now associated to pin 1. Figure 18-13 presents the final result.

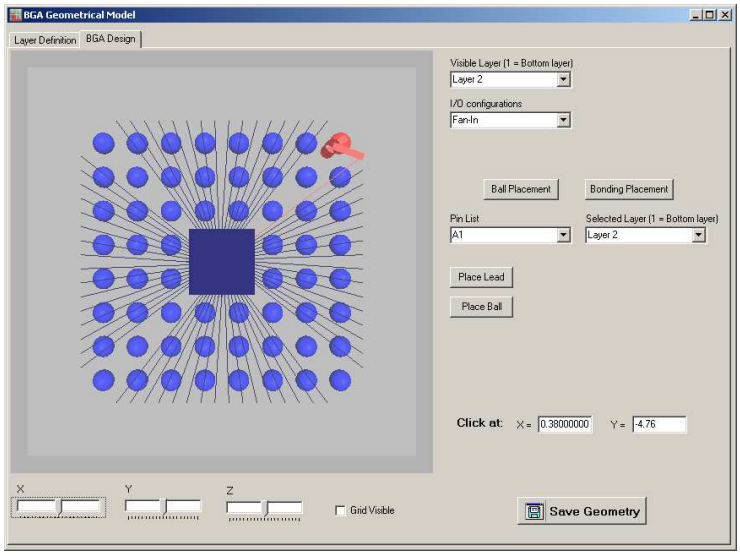


Figure 18-13 : Design of pin A1 (package\test_BGA.geo)

Do the same for all the pins of the package. At the end, click on the button “Save Geometry”. The screen is closed and you return to the Advanced Package Extraction Tool to view the geometrical model and compute electrical partial elements. In order to present an example of a complete BGA model built with this tool, open the file “package\BGA64_model.geo”. This file describes the geometrical model of the BGA 64 presented in the 2.4 part of the Getting started chapter. Figure 18-14 presents the geometrical model. The internal routing of the BGA was built from a X-ray view of the package. Figure 18-15 presents the simulation result of the partial inductance.

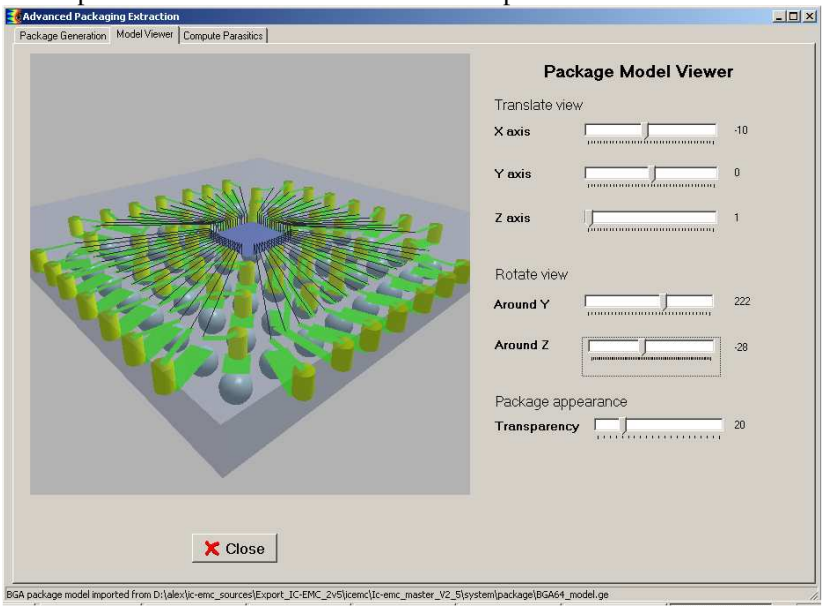


Figure 18-14 : Constructed model of a BGA 64 (package\ BGA_model.geo)

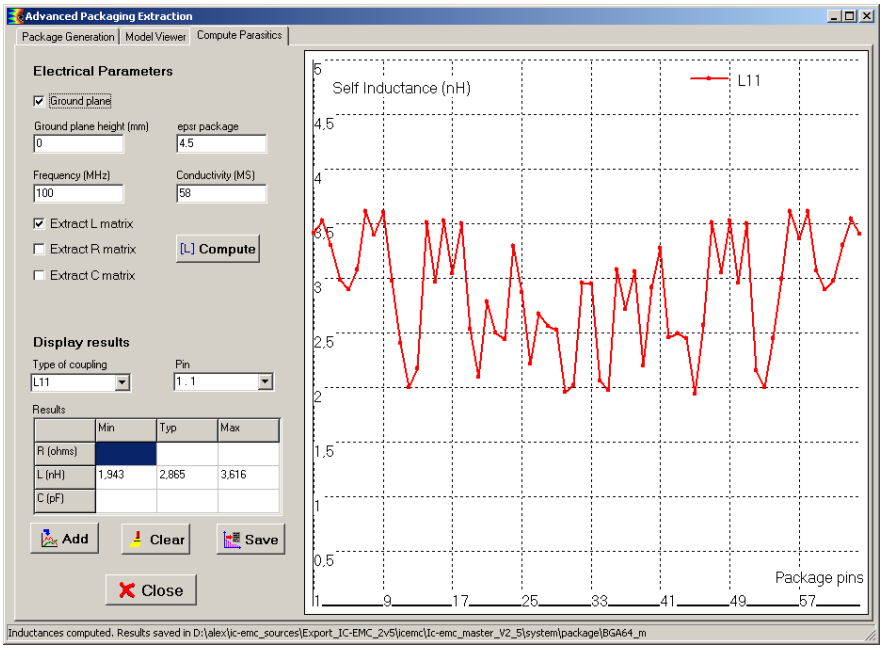


Figure 18-15 : Simulated partial inductance of a BGA 64 (package\ BGA_model.geo)

18.5 References

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19 Notations and Constants

19.1 Notations

Value	Name	Standard Notation
10^{18}	PETA	P
10^{15}	EXA	E
10^{12}	TERA	T
10^{9}	GIGA	G
10^{6}	MEGA	MEG (in SPICE)
10^{3}	KILO	K
10^{0}	-	-
10^{-3}	MILLI	m
10^{-6}	MICRO	u
10^{-9}	NANO	n
10^{-12}	PICO	p
10^{-15}	FEMTO	f
10^{-18}	ATTO	a
10^{-21}	ZEPTO	z

19.2 Physical constants and parameters

Name	Value	Description
ε_0	8.85 e $^{-12}$ Farad/m	Vacuum dielectric constant
ε_r SiO_2	3.9 - 4.2	Relative dielectric constant of SiO_2
ε_r Si	11.8	Relative dielectric constant of silicon
ε_r ceramic	12	Relative dielectric constant of ceramic
k	1.381e^{-23} J/°K	Boltzmann constant
q	1.6e^{-19} Coulomb	Electron charge
μ_n	600 V.cm^{-2}	Mobility of electrons in silicon
μ_p	270 V.cm^{-2}	Mobility of holes in silicon
γ_{al}	36.5 10^{6} S/m	Aluminum conductivity
γ_{si}	4x10^{-4} S/m	Silicon conductivity
n_i	1.02x10^{10}cm^{-3}	Intrinsic carrier concentration in silicon at 300°K
ρ_{al}	0.0277 Ω.µm	Aluminum resistivity
γ_{cu}	58x10^{6} S/m	Copper conductivity
ρ_{cu}	0.0172 Ω.µm	Copper resistivity
$\rho_{tungstène\ (W)}$	0.0530 Ω.µm	Tungsten resistivity
$\rho_{or\ (Ag)}$	0.0220 Ω.µm	Gold resistivity
μ_0	1.257e^{-6} H/m	Vacuum permeability
T_0	300°K (27°C)	Operating temperature

20 Glossary

BGA	Ball Grid Array
CMOS	Complementary Metal Oxyde Silicium
DPI	Direct Power Injection (IEC 62132-4)
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESL	Equivalent Serial Inductance
ESR	Equivalent Serial Resistor
FFT	Fast Fourier Transform
I/O	Input Output
IA	Internal Activity (ICEM terminology)
IBIS	I/O Buffer Information Specification
IC	Integrated Circuit
ICEM	Integrated Circuit Emission Model (IEC 62433-2)
ICIM	Integrated Circuit Immunity Model (IEC 62433-4)
PCB	Printed Circuit Board
PDN	Power Distribution Network, or Passive Distribution Network (ICEM terminology)
PEEC	Partial Element Equivalent Circuit
PLL	Phase Locked Loop
PWL	Piece Wise Linear
QFP	Quad Flat Package
RFI	Radio Frequency Interference
SPICE	Simulation Program with Integrated Circuit Emphasis
SSN	Simultaneous Switching Noise
TDR	Time Domain Reflectometry
TEM	Transverse Electromagnetic
VNA	Vector Network Analyzer

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